A Fast Digital Phase Frequency Detector with Preset Word Frequency Searching in ADPLL for a UHF RFID Reader

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Abstract-An All-Digital Phase-Locked Loop (ADPLL) is an architecture that is widely employed in the communication system due to the advancement of the Complementary Metal-Oxide-Semiconductor (CMOS) technology process. A 2.4GHz Radio Frequency Identification (RFID) system needs a frequency synthesizer in the local oscillator architecture of the transceiver to generate a stable frequency tuning range Therefore, in this paper, a Digital Phase-Frequency Detector (DPFD) is designed to achieve the phase and frequency acquisition in the ADPLL system. The proposed DPFD is divided into two main parts, the first is the Phase Detector (PD) and the second is the Frequency Detector (FD). The PD has managed to detect the presence of the phase difference by recognizing two different input signals. The FD, on the other hand, is capable to detect the higher frequency by identifying the output signals from the PD in digital formation. In addition, a control unit module is developed to control and adjust the Preset Word (PW) for the system by using a binary search scheme. Comparison results show that the final value of the PW from the simulation is the same as from the manual calculation (theoretical values). The digital PFD and the PW control modules are designed and simulated by using Verilog HDL code. These two designed modules will be integrated into the targeted ADPLL to achieve fast locking performance and ultra-low power for Ultra-High Frequency (UHF) RFID applications.

Keywords-RFID; all-digital PLL; ADPLL; digital PFD; frequency synthesizer; local oscillator; binary search

I. INTRODUCTION

Internet-of-Things (IoT) is a main component of the application system of a smart city. Radio Frequency Identification (RFID) is one of the integration applications that work with the IoT that is widely employed in the biomedical and healthcare industries. With the IoT, we can monitor a patient's health such and observing his severe or chronic disease [1] and tracking medical members and properties through smart application devices by using Wireless Sensor Network (WSN) nodes [2, 3] or RFID tags that are connected to the server. RFID is a system that aims to exchange identification information or data from the tag to the RFID reader through an RF transceiver antenna [4] to carry out specific applications based on the data stored in the tag [5]. Presently, RFID technology system devices have been developed to accommodate low-power devices with enhanced data transfer capabilities [6].

Figure 1 depicts the typical transceiver of the 2.4GHz RFID reader and includes some basic blocks such as an RF antenna, a receiver block, a transmitter block, a switch, and a Local Oscillator (LO). In the transceiver, the LO plays a crucial role in the architecture by providing the tuning frequencies for the transmitter and the receiver. Furthermore, in the 2.4GHz applications, a frequency synthesizer is required to produce a varying high-frequency range of the LO. PLL is commonly used in the frequency synthesizer. Based on the literature, the PLL is built either in analogue, mixed-analogue-digital, or fully digital. In the analogue PLL, the configuration typically consists of a Voltage-Controlled Oscillator (VCO), a Phase-Frequency Detector (PFD), an analogue Loop Filter (LF) [7] or a charge-pump loop filter [8], and a fractional divider at the feedback loop. Nevertheless, the trend of implementing the digital circuitry using the Very Large-Scale Integration (VLSI) is gradually increased due to the advancement of the CMOS technology process because of its advantages over the analogue counterparts [9], such as the fast acquisition of the phase and the frequency, the smaller size, and the low power

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consumption. Besides, the ADPLL has a better performance of a less complex design, better jitter, high stability, and good locking-in time [10].

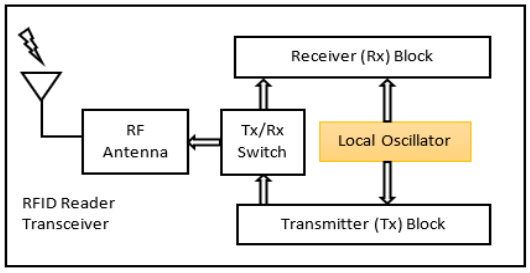

Fig. 1. RFID reader transceiver.

Currently, the advanced transceiver's requirement no longer can be met by the analogue PLL [11] because the analogue parts in the PLL are very sensitive to a wide range of design constraints as compared to the digital parts. For instance, the operating DC bias voltage shifts, the challenge of building Higher Order Filters (HOFs), the requirement for the initial and the recurring calibration for the devices, etc. [12]. On top of that, due to its low mobility process, the analogue part is typically difficult to reuse across process technologies. Nearly every analogue part needs to be modified or redesigned, and more advanced technology requirements to be implemented or imported for the sake of cost saving or performance enhancement. Furthermore, the fabrication of the analogue or mixed-analogue-digital devices is typically more expensive since the capacitors required for the analogue circuits require additional processing procedures. Thus, the transition of the analogue or mixed-analogue-digital PLL to the ADPLL gradually increases. The ADPLL is more desirable in deep submicron process technology and it is also much preferred in the RFID application system. It is because of the advancement of digital over analogue circuits in lower voltage operation and higher tolerance to the on-chip noise, where the low supply voltage and high noise immunity are very demanding [13-15]. The Process, Voltage, and Temperature (PVT) variations [16] form one crucial issue in the ADPLL design, especially in settling the time performance. However, the pre-setting and the estimating oscillator tuning word technique as introduced in [16, 17] may solve the PVT issue. Moreover, the voltage variation in the DCO can be reduced by the supply noise cancellation technique [18, 19]. This shows that the ADPLL design is robust.

Some research works on the fast-locking techniques have been reported. The authors in [17] improved the locking process in their proposed ADPLL system by improving the Oscillation Tuning Word (OTW) using the estimation and pre-set technique and the frequency search is utilizing one by one step. In [12, 13, 20] the frequency search is defined by a binary search scheme. Both techniques are reliable to be implemented in future design but in terms of the fast-locking performance, the binary search scheme is preferred. In this paper, the digital phase and frequency detector designs are presented in the first part. In the second part, the PW for the DCO operation will be investigated and discussed.

II. ADPLL ARCHITECTURE

The ADPLL architecture is constructed with a Digital Phase-Frequency Detector (DPFD), a Control Unit (CU), a DCO, and a divider at the loop feedback as can be seen in [21]. The DPFD is an important part of the ADPLL architecture which determines the difference and mismatch of the phase and frequency of two input signals, namely the frequency reference signal and the divided DCO output frequency signal. The DPFD has been redesigned and restructured by many researchers [12, 22-25] to achieve fast detection and acquisition performance in ADPLL. The Time-to-Digital Converter (TDC) is a famous design architecture for developing a DPFD. It has good measurement capabilities for the time difference between the edge of the two input signals [26] and it also performs well in terms of resolution [27]. Reviews have been conducted in [28] about the phase-frequency detector in various ADPLL design topologies. In [24], the use of a bang-bang PFD in ADPLL is quite attractive due to the better phase locking-in time, good jitter performance, and small area as compared to the use of the full-ranged TDC. In addition, the calibrating process is needed in the ADPLL design [24] to minimize the quantization noise if the TDC is used in the design. In this paper, the Phase Detector (PD) and Frequency Detector (FD) as DPFD and frequency searching by using a bisection scheme are proposed to achieve fast locking detection in ADPLL.

III. CIRCUIT IMPLEMENTATION

A. Proposed Phase Detector Design

In this part, a new design of a PFD is proposed, which combines the phase and the frequency block to accomplish fast acquisition performance, as shown in Figure 2. This is an extension work from [21], but major improvements have been made. The proposed design comprises two main parts: the PD and the FD. The output of this PFD will be converted into digital form.

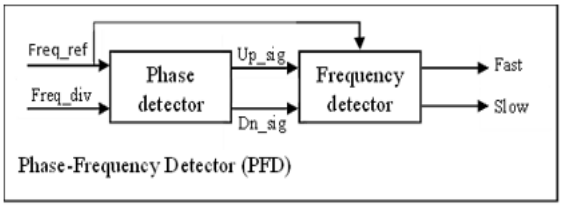

Fig. 2. The proposed DPFD design.

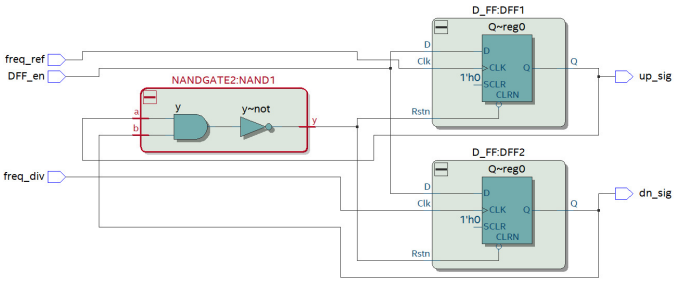

Fig. 3. Logic diagram of the PD.

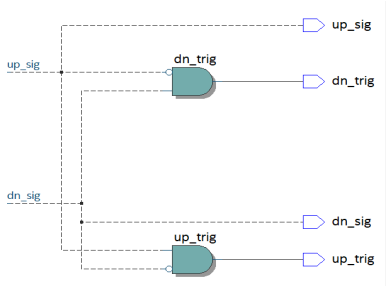

Fig. 4. The logic diagram to overcome a dead zone in PD.

The PD design in this work is adapted from [21], consisting of two D-flip-flops and a NAND gate at the feedback. This configuration design is chosen due to the dead zone problem, and it is quite a famous design in phase error detection between the reference signal clock and the divided DCO signal clock. Based on Figure 3, the PD block detects two input signals: the reference frequency clock (freq_ref) and the divided DCO frequency clock (freq_div). The PD block generates the output signals that are called up_sig and dn_sig. In the initial state, both up_sig and dn_sig pulses are zero until either the positive edge of freq_ref or freq_div is received. The output of up_sig will be triggered if the PD detects the positive edge of freq_ref is leading the freq_div. On the other hand, the production of dn_sig will be triggered if the PD detects the opposite operation. The logic diagram in Figure 4 is the extension circuit of the proposed PD design. This circuit is added to eliminate the dead zone pulses that produced from the logic diagram in Figure 3. The purpose of the added circuit is to produce a stable output for the controller block in the next work. This circuit also generates output signals namely up_trig and dn_trig.

B. Modified Frequency Detector Design

The other part of the proposed PFD block is the FD. The FD in this work is an improved design based on the previous work of [21] as illustrated in Figure 5. It receives the signal of up_trig and dn_trig from the previous PD block that synchronizes with the reference frequency clock and produces two exclusive outputs of "slow" and "fast" signals. The proposed FD is constructed utilizing the frequency comparison technique as described in [10], whereby a comparator is employed to compare two generated signals and produced two output signals. Figure 6 depicts the proposed design's flowchart for the frequency acquisition step. It is aimed to lock the DCO target frequency to the reference frequency clock by ignoring the phase recognition. As soon as the system starts, all variables are set to zero and the counters are assigned for the reference clock, the up_trig, and the dn_trig. After that, the inputs reference clock, up_trig, and dn_trig go through a counting process. At the 14^{th} cycle of the reference clock, the signal of the "complete clock" will be activated, allowing the system to do comparisons between the up_trig and the dn_trig. In this comparison process, the system will be checking the output counter for both up_trig and dn_trig. If the system detects the counting of up_trig is more than dn_trig, the "fast" signal will be activated, wjile if the opposite operation is detected, the "slow" signal will be triggered.

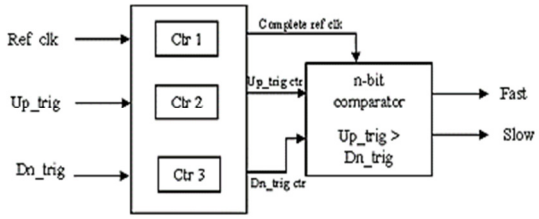

Fig. 5. The proposed FD design block diagram.

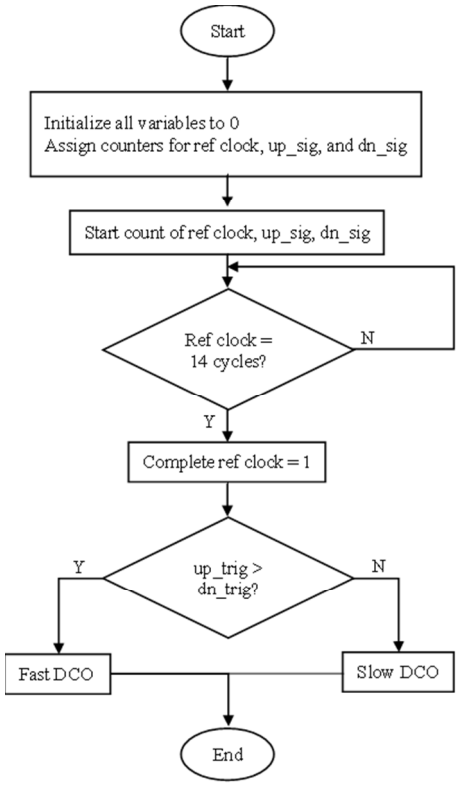

Fig. 6. FD design flowchart.

Therefore, three counters (Ctr1, Ctr2, Ctr3) are employed to count the frequency cycles of the three input signals to execute the frequency acquisition step. Ctr1 is used to track the reference frequency clock, while the other two counters (Ctr2 and Ctr3) are used to count up_trig and dn_trig pulses. Additionally, the proposed FD includes an n-bit comparator, which compares the output of the two counters from up_trig and dn_trig and as a result, generates the "fast" and "slow" signals. In further development, the DCO will be operated via two of these output signals. The definition of "fast" and "slow" correspond to the accelerating and the decelerating of the operation frequency at the DCO, respectively.

C. Control Unit

A CU is another approach to filter the bit control in the ADPLL instead of using the Digital Loop Filter (DLF). There are many considerations in designing the DLF to achieve fast locking performance, such as by considering a proper loop gain selection for the gain controller [25], a dynamic filter bandwidth adjustment [29, 30], a voltage buffer amplifier, etc. and these make the design complex and unstable. Hence, to

overcome these problems, a CU design is chosen because of the advantages of a simpler and a more stable design as compared to the DLF. A CU is a module that can change the PW of the DCO adjustment operation frequency to achieve fast locking performance. There are two methods to lock the PLL, first, the locking time approach in digital PLL, as shown in Figure 7, introduces gradual frequency changes until the target frequency is reached. This search type is a simple search scheme, but it takes a long time to lock the phase and frequency of the ADPLL. The second approach is by using a binary search scheme. It is a fast-searching algorithm, where the frequency changing process depends on certain rules or conditions and is quite popular and used in many research works. Many binary scheme approaches have been reported, but the method in [31] is more attractive for the PW value calculation because of the successful lock-in time reduction of 80-90% in the design. The design searches the target frequency by using the bisection scheme in the PW calculation. The frequency changing process is shown in Figure 8. The binary search performs faster-locking time process in ADPLL as compared to the linear frequency search.

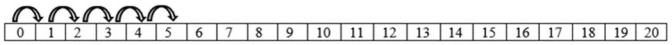

Fig. 7. Linear or sequential frequency search.

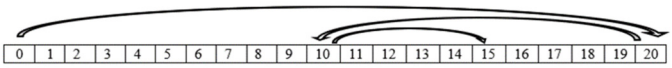

Fig. 8. Binary frequency search.

In this work, the PW calculation is adjusted using the bisection scheme which is an iteration process that determines the estimated roots from a given range of values [32]. To realize the operation of the bisection scheme, the maximum and the minimum frequency determination should be initialized. According to Figure 8, it is assumed that the frequency control has 21 words, including the word 0. If the target frequency is increased, the PW would be increased by half and vice versa. The equation of the bisection scheme can be written as follows:

When the target frequency increases:

$$f_{dco}^{n+1} = f_{min} + \frac{f_{max} - f_{min}}{2} \quad (1)$$

where $f_{min} = f_{dco}^{n}$.

When the target frequency decreases:

$$f_{dco}^{n+1} = f_{max} + \frac{f_{max} - f_{min}}{2} \quad (2)$$

where $f_{max} = f_{dco}^{n}$.

In (1)-(2), f_{dco}^{n+1} is the frequency control word for the next state, and f_{dco}^{n} is the frequency control word for the current state.

The increase or the decrease in target frequency is a rule condition of the system that is produced by our digital PFD. Moreover, the increase in target frequency represents the "fast" signal that is triggered in the FD, while the decrease in target frequency represents the "slow" signal that is produced by the FD. However, to program the equation as in (1) and (2) into our ADPLL system by using the Verilog HDL code is very tricky due to the division operator. Thus, the equations are reformed as follows:

When the "fast" signal is triggered:

$$PresetWord_{n+1} = PresetWord_n + PWspan \quad (3)$$

When the "slow" signal is triggered:

$$PresetWord_{n+1} = PresetWord_n - PWspan \quad (4)$$

where $PresetWord_{n+1}$ is the frequency control word for the next state, and $PresetWord_n$ is the frequency control word for the current state.

IV. Simulation Results and Analysis

The simulations in this paper are conducted using the Verilog HDL code and they are divided in three parts: the PD simulations, the FD simulations, and the PW calculations simulations.

A. PD Simulations

The PD simulations are conducted in two operations: A) Freq_ref is faster than Freq_div, and B) Freq_ref is slower than Freq_div. The simulation setup for A and B are set as follows:

- A: Reference frequency = 40MHz, assumed DCO divided frequency = 35.7MHz.
- B: Reference frequency = 40MHz, assumed DCO divided frequency = 43.48MHz.

Figure 9 shows the timing diagram of the PD block in this work. The circuit in Figure 4 is added to the PD block to minimize the dead zone problem to produce a stable system indicated as 1 in Figure 10. The new output signals of the PD are produced and named up_trig and dn_trig. After the circuit in Figure 5 is added to the PD design, the dead zone signal is removed from the system indicated as 2 in Figure 9.

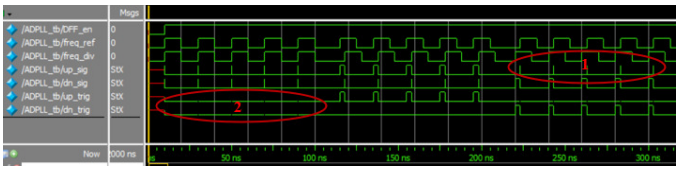

Fig. 9. Simulation result of the circuit in Figure 4 added into the PD.

Figures 10 and 11 show the simulation results for the two setups. The results show that the up_trig signal goes up when the freq_ref signal is faster than the freq_div and the dn_trig signal goes up when the freq_div is faster than the freq_ref. Both up_trig and dn_trig signals are presented as pulse signals. The pulse width (w_{pulse}) for the up_trig and dn_trig signals represent the phase differences or phase error ($\emptyset_{error}$) between the freq_ref and the freq_div. The relationship between the pulse width for up_trig and dn_trig is directly proportional to the phase error as shown in (5), where the smaller the pulse width of up_trig and dn_trig, the smaller the phase error between the freq_ref and the freq_div.

$$w_{pulse} \propto \emptyset_{error} \quad (5)$$

The second stage output for both results is presented as up_trig and dn_trig. The results clearly show that the strike pulse at the first stage output has no longer appears at the second stage output. Therefore, the proposed PD in this work achieved a stable signal for the frequency detection.

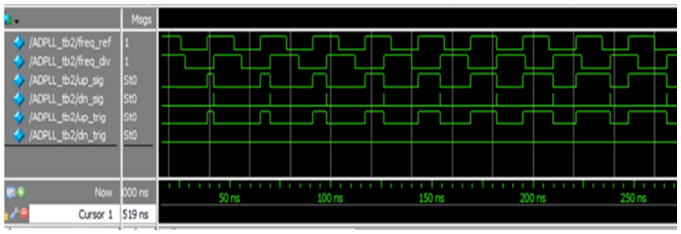

Fig. 10. The simulation result for freq_ref is faster than freq_div.

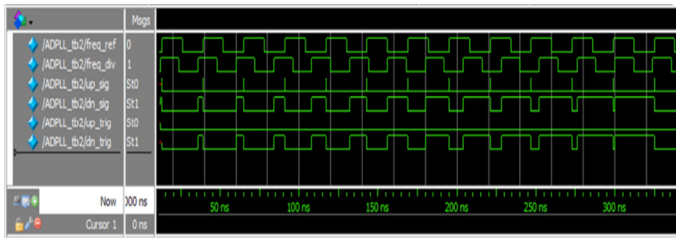

Fig. 11. The simulation result for freq_div is faster than freq_ref.

B. FD Simulations

The FD simulations are conducted in two operations. The first operation is set up for when freq_ref is faster than freq_div and the second operation is set up for when freq_div is faster than freq_ref. For this part, the FD design is integrated with the PD design by using the Verilog HDL code. The RTL view of the circuit is shown in Figure 12. The simulation frequencies setup is the same as in the previous part. Figure 13 shows the simulation result for freq_ref faster than freq_div while the simulation result in Figure 14 shows the situation when freq_ref is slower than freq_div. It should be noted that the system for this part will compare the frequency of the freq_ref and freq_div without taking into account the phase alignment but only taking into account the pulses of the output signal frequency. The output pulses will be counted and the system will compare which counter will produce the highest value. In Figure 13, the system detects that the frequency of up_trig pulses is higher than dn_trig pulses through the output counter. According to the flowchart in Figure 6, when the up_trig pulses produce the higher one, the system will send the "fast" signal to the DCO. Thus, the "fast" signal is triggered in Figure 13 after the signal of counting freq_ref is completed, while in Figure 14, the opposite operation is detected and the dn_trig count pulses are higher than the up_trig-count pulses. In this situation, the "slow" instruction will be sent to the DCO. Based on the FD simulation results, the fast detection performance is achieved because of the FD system can complete at thirteenth cycles of the freq_ref.

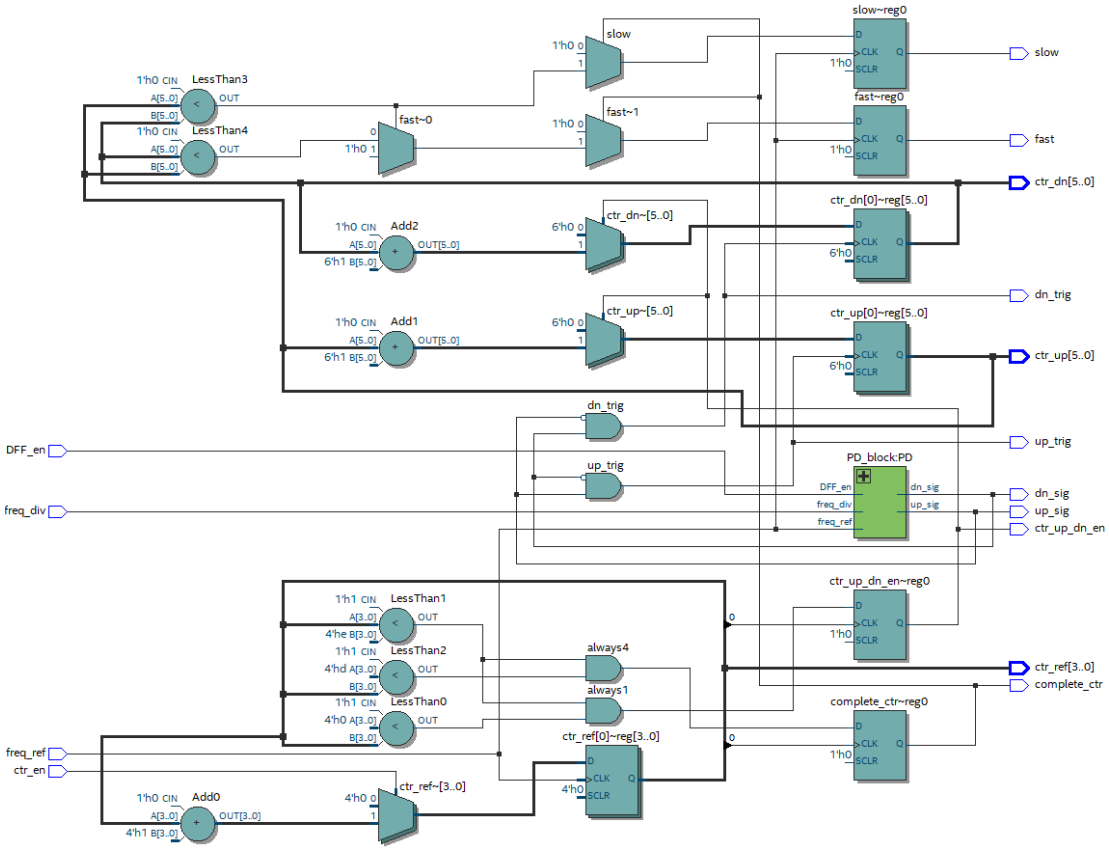

Fig. 12. The RTL view for PD and FD design architecture in Verilog HDL.

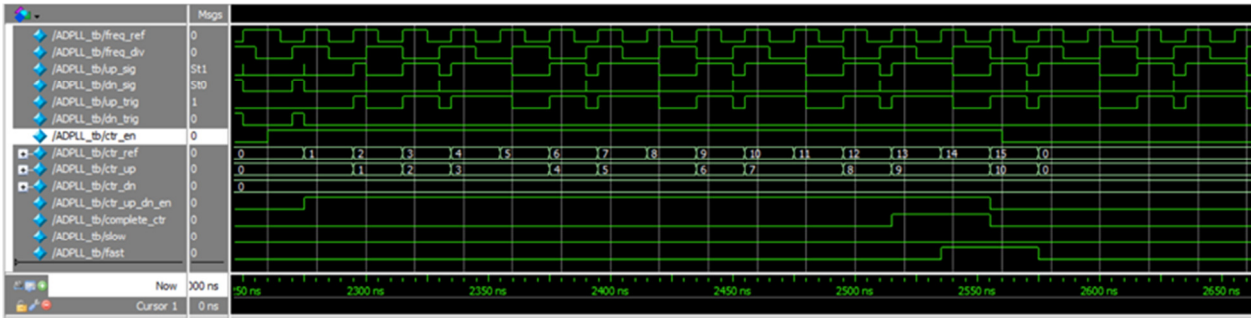

Fig. 13. The simulation result for FD design when up_trig pulses are higher than dn_trig pulses.

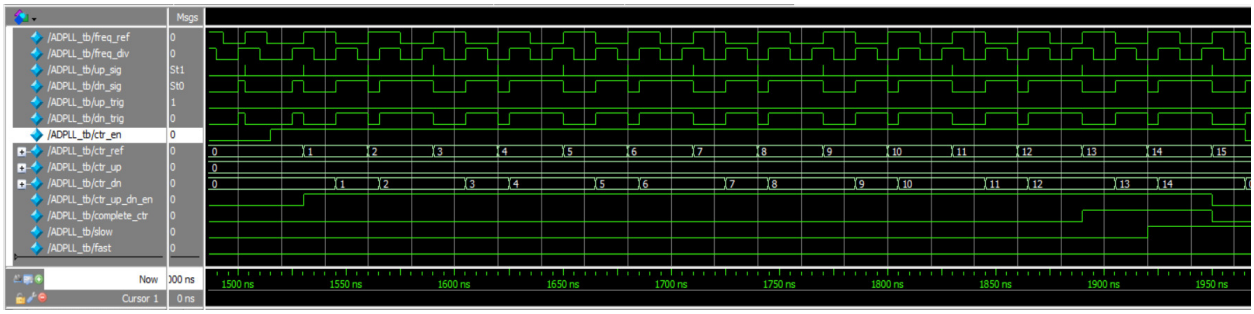

Fig. 14. The simulation result for FD design when dn_trig pulses are higher than up_trig pulses.

TABLE I. SUMMARY OF THE PW USING MANUAL CALCULATIONS FOR THE PROPOSED SYSTEM

Input									**Output**								
1	2	3	4	5	6	7	8	9	PW1	PW2	PW3	PW4	PW5	PW6	PW7	PW8	Final_PW
0	0	0	0	1	1	1	0	1	159	239	279	299	289	284	281	282	281
0	0	0	1	1	1	0	0	0	159	239	279	259	249	244	246	247	248
0	1	1	1	0	1	1	1	1	159	79	39	19	29	24	21	20	19

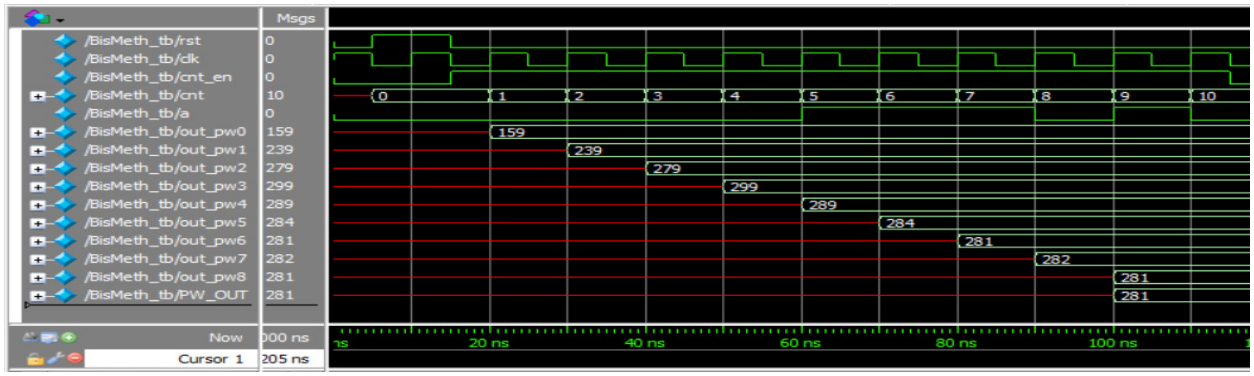

Fig. 15. System testing for input 000 011 101.

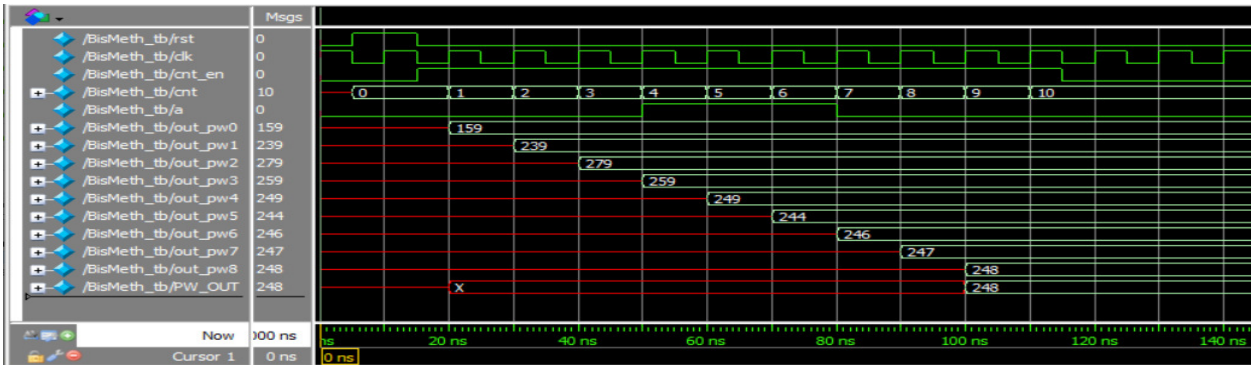

Fig. 16. System testing for input 000 111 000.

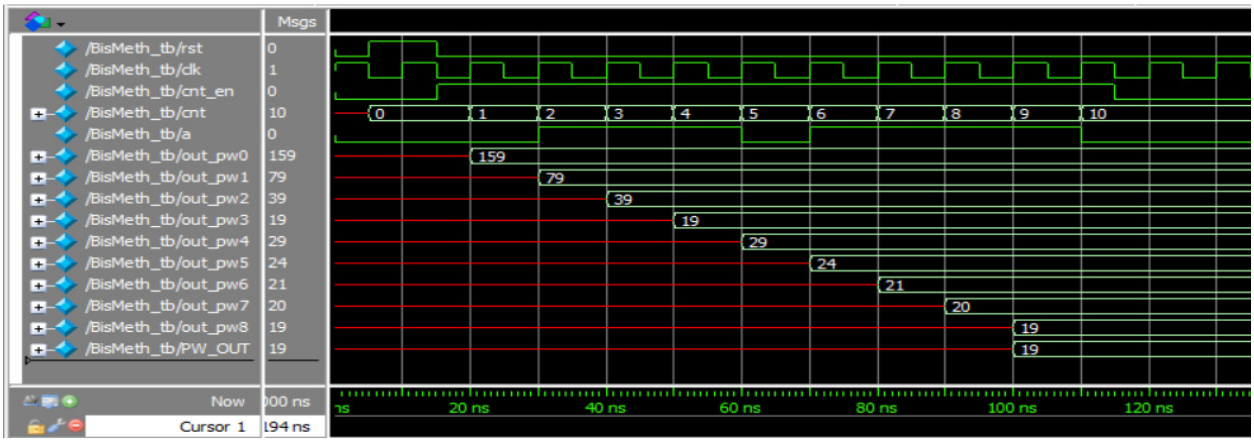

Fig. 17. System testing for input 011 101 111.

C. Simulations of the PW Calculations

In this work, the module of PW calculations is presented using the Verilog HDL coding. The system receives the signal from the PFD block, which is a "slow" or "fast" signal. Nevertheless, in the testing platform, the "slow" and "fast" signals are represented as a binary form of 0 and 1 respectively. The manual calculation of the PW for the proposed system is presented in Table I. Only 3 tests are shown in this section to prove that the proposed system produces the same output as the theoretical values. Nine detections of input are developed in the system. When the system detects the binary 0, the PW is increased and when the binary 1 is detected, the PW is decreased. There are also 9 PW outputs presented and the 9th detection is the last detection, which produced the final PW for the DCO operation. Figures 15 - 17 show the simulation results for the testing input of 000 011 101, 000 111 000, and 011 101 111 respectively. Based on the PW shown at the bottom list for each Figure, the values are matched with the manual calculation as in Table I. Thus, the proposed design shows that the PW searching is achieved very fast and only takes 9 cycles to calculate the desired value. Based on the proposed design, the good results of the PD and the FD simulation and the PW searching are presented. In this work, the dead zone problem is considered in order to achieve the phase acquisition step and system stability.

The dead zone occurs when the PFD is unable to distinguish the phase mismatch of the positive or the negative edges of the two input signals and it may lock to the incorrect phase [33]. The incorrect phase-locked may degrade the phase noise performance. Thus, to achieve better phase acquisition performance, the proposed PD design architecture has successfully removed the dead zone pulses as presented in [34]. Furthermore, the proposed FD design has adopted the frequency acquisition step technique to achieve locking mechanism and system accuracy. Our proposed FD is able to count and compare the frequency pulses of each signal directly. Our design improved the PFD block of the work of [31] where their ADPLL did not consider the frequency acquisition step.

Next, the PW frequency searching in the proposed work is to achieve the target frequency and it is based on the binary search algorithm and the changing frequency step of the proposed PW is using a bisection scheme calculation. In our PW design, the large frequency step takes place in the early PW calculation, and it saves a lot of time to reach the target frequency which takes only 9 steps for 320 frequency control codes. Our frequency searching is simpler as compared to using the oscillator tuning word (OTW) algorithm in [16, 35].

V. CONCLUSION

A digital PFD for the RFID-ADPLL architecture is proposed and designed in this paper with the Verilog HDL system. The design of the PFD is divided into two main parts, which are the phase-detection and frequency-detection to achieve the phase acquisition and the frequency acquisition respectively. The proposed PD module consists of two components of D-flip-flop and a NAND gate at the reset feedback. The outputs of the up_trig and dn_trig signals are well-produced by eliminating the dead zone signal and presented a stable output for the FD module. In addition, the FD module is designed by comparing the counting value of the up_trig and the dn_trig signals. As a result, the "fast" and "slow" signals are produced at the thirteenth cycle of freq_ref and represent the increase and decrease of the operation of the future DCO respectively. Moreover, to search the target frequency for the DCO, a binary search scheme is used to calculate the PW for controlling the DCO operation in the future. The manual calculation of the PW has also been tabulated for the theoretical comparison. The comparison shows that the PW calculation in simulations is matched with the theoretical values and finished the calculation at the nineth cycle detection of freq_ref. Based on the results of the DPFD and the PW searching, fast detection performance is achieved in this work. In future research work, the control code output generated from the proposed digital PFD and the PW searching will be connected to the DCO block

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