4×4-Bit Array Two Phase Clocked Adiabatic Static CMOS Logic Multiplier with New XOR

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Abstract— **This paper presents the simulation results of a 4×4-bit array two phase clocked adiabatic static CMOS logic (2PASCL) multiplier using 0.18 μm standard CMOS technology. We also propose a new design of 2PASCL XOR which reduces the number of transistors as well as the power consumption. Analytical method to compare the lower current flow in adiabatic circuit is also presented. At transition frequencies of 1 to 100 MHz, 4×4-bit array 2PASCL multiplier shows a maximum of 55% reduction in power dissipation to that of a static CMOS. The results indicate that 2PASCL technology can be advantageously applied to low power digital devices operated at low frequencies, such as radio-frequency identifications (RFIDs), smart cards, and sensors.**

I. INTRODUCTION

In recent years, various energy recovery circuits with adiabatic circuitry for ultra-low power implementation have been presented [1]–[15]. Adiabatic charging [1] is a principle where all charge transfer occurs without generating heat. The energy advantage can be understood by assuming a constant current source that delivers the charge $C_L V_{dd}^2$ over a time period T. The dissipation through the channel resistance R is then $E_{diss} = (\frac{RC_L}{T})C_L V_{dd}^2$ [2]. Theoretically, it is possible to reduce the dissipation to an arbitrary degree by increasing the switching time to ever-larger values. Conventional adiabatic logic circuits [1]–[10] that have been proposed shows a much less power dissipation compared with static CMOS circuit. For instance, at 10 MHz clock input, efficient charge recovery logic (ECRL) [10] dissipates only 16% of the energy of static CMOS logic in a chain inverter application. However, most of these circuits require multiphase power clocks. Several problems, such as a complicated clock design and an increase of energy dissipation due to the power clocks occur. Furthermore, for a single and a two phase clock circuits, diode-based families [4]–[9] have several disadvantages such as output amplitude degradation and the energy dissipation across the diodes in the charging path [16].

At the earlier stage of the 2PASCL [17], we have designed, simulated, and compared the power consumption of 2PASCL NOT, 2NAND, 2XOR, and 2NOR to CMOS topology. We have also discussed the pros and cons of 2PASCL compared to other proposed adiabatic logics that are easily derived from CMOS in [16]. 2PASCL fundamental logics significantly exhibit a lower power dissipation [18]–[19].

In this paper, we simulate a 4×4-bit array 2PASCL multiplier utilizing 0.18 μm standard CMOS technology using a new 2PASCL 2XOR. Analysis on the low-power dissipation in adiabatic charging and discharging using constant voltage value and ramp-wave voltage is also carried out. 2PASCL technology can be advantageously applied to low power digital devices operated at low frequencies, such as radio-frequency identifications (RFIDs), smart cards, and sensors.

The remainder of the paper is organized as follows. Section II describes the adiabatic charging theory. In Section III, we briefly explain the circuit operation of 2PASCL. In Section IV, the simulation results of 2XOR and 4×4-bit array 2PASCL multiplier are presented. Section V includes concluding remarks and future work.

II. ADIABATIC CHARGING

Adiabatic charging is the technique in which charge moves from power supply to the load capacitance by using slow and constant-current charging. This can be modeled by analytically deriving the current i_p (current flow through pMOS) of instant V_{dd} and ramp wave from V_ϕ, the voltage supply as shown in Fig. 1.

The i_p equation can be derived as below;

$$V_\phi(t) = R_p i_p(t) + v_y(t), \tag{1}$$

$$i_p(t) = C\frac{dv_y(t)}{dt}, \tag{2}$$

$$v_y(0_-) = 0, \tag{3}$$

for constant V_{dd};

$$V_\phi(t) = V_{dd}, \tag{4}$$

therefore,

$$i_p(t) = \frac{V_{dd}}{R_p}e^{-\frac{t}{RC}}, \tag{5}$$

for ramp-wave voltage;

$$V_\phi(t) = \frac{V_{dd}}{\tau}t\left[u(t) - u(t-\tau)\right] + V_{dd}\left[u(t-\tau)\right], \tag{6}$$
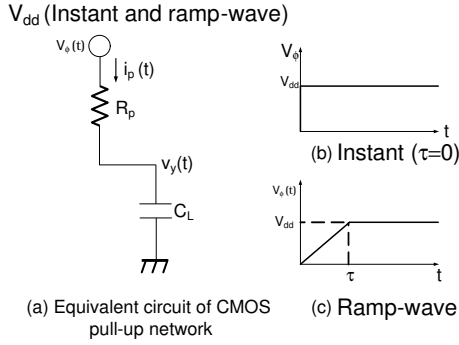
therefore,

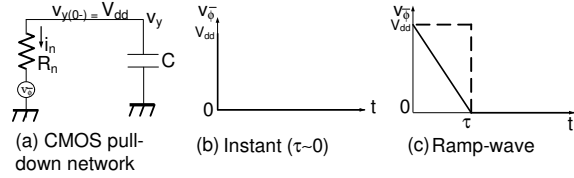Fig. 1.   CMOS equivalent circuit during pull-up network.

Fig. 2.   CMOS equivalent circuit during pull-down network.

$$i_p(t) \quad = \quad \frac{CV_{dd}}{\tau}(1 - e^{\frac{-t}{CR_p}}) - \frac{CV_{dd}}{\tau}(1 - e^{\frac{t-\tau}{CR_p}})u(t-\tau), \quad (7)$$

where, $u(t)$ denotes Heaviside's unit function.

From Eq. (7), it is clearly seen that i_p can be reduced by increasing τ, the time for V_ϕ to change from 0 to V_{dd}.

As shown in the equivalent circuit of CMOS during pull-down network as in Fig. 2, i_n can be derived as below;

$$0 \quad = \quad R_n i_n(t) + v_y(t), \quad (8)$$

$$i_n(t) \quad = \quad -C\frac{dv_y(t)}{dt}, \quad (9)$$

$$v_y(0_-) \quad = \quad V_{dd}. \quad (10)$$

for adiabatic discharging,

$$V_{\overline{\phi}}(t) \quad = \quad V_{dd} - \frac{V_{dd}}{\tau}t\left[u(t) - u(t-\tau)\right], \quad (11)$$

therefore,

$$i_n(t) = V_{dd}\left[R_n C^2 + \frac{1}{\tau}\left[-(CR_n + t - e^{\frac{t-\tau}{R_n C}}(\tau + CR_n))\right.\right.$$
$$\left.\left. u(t-\tau) + \tau(-1 + e^{\frac{t}{CR_n}}(1 - CR_n) + t)\right]C\right]. \quad (12)$$

From Eq. (12), it is also demonstrated that i_n can be reduced by increasing τ, the time for V_ϕ to change from V_{dd} to 0.

III. 2PASCL

A. Circuit Operation

Figure 3 shows a circuit diagram and waveforms illustrating the operation of the 2PASCL inverter [17]. Waveforms of Fig. 3 (b) are the input, split-level sinusoidal power supply
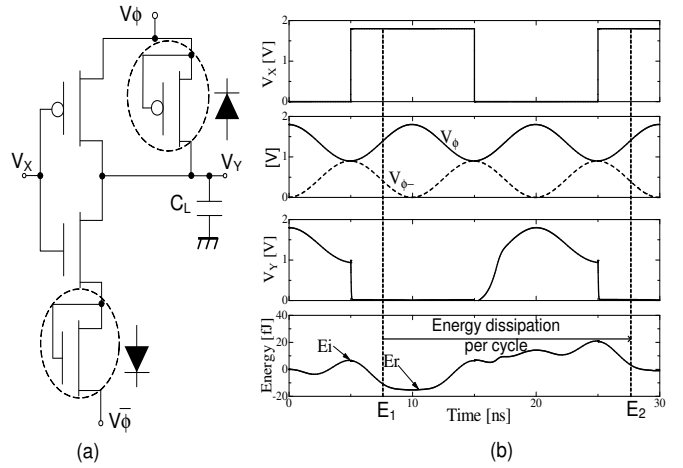

Fig. 3.   (a) 2PASCL inverter circuit. (b) Waveforms from the simulation, transition frequency X=50 MHz, $V_\phi = V_{\overline{\phi}}$ = 100 MHz.

TABLE I
2PASCL NOT LOGIC CIRCUIT OPERATION

Mode	Y_{-1}	pMOS	nMOS	Y
Evaluation	LO	ON	OFF	HI
	HI	OFF	ON	LO
Hold	HI	OFF	ON	No Transition

clocks and the output. The power supply clocks used in 2PASCL are V_ϕ and $V_{\overline{\phi}}$, where

$$V_\phi \quad = \quad \frac{V_{dd}}{4}\sin(\omega_o t + \theta) + \frac{3}{4}V_{dd}, \quad (13)$$

$$V_{\overline{\phi}} \quad = \quad -\frac{V_{dd}}{4}\sin(\omega_o t + \theta) + \frac{1}{4}V_{dd}. \quad (14)$$

On the last graph of Fig. 3(b), the instantaneous energy dissipation is presented. In energy-recovery circuits, based on the energy conservation law, energy dissipated is equal to the total of energy injected to the circuit, E_i and the energy received back from the circuit capacitance, E_r. This is shown in this energy dissipation graph.

The circuit operation is divided into two phases, *evaluation* and *hold*. In the *evaluation* phase, V_ϕ swings up and $V_{\overline{\phi}}$ swings down. On the other hand, in the *hold* phase, $V_{\overline{\phi}}$ swings up and V_ϕ swings down. Let us consider the inverter logic circuit demonstrated in Fig. 3. The operation of the 2PASCL inverter can be summarized as in Table I.

The number of dynamic switching transition occuring during the operation of the 2PASCL circuit decreases since the charging/discharging of the circuit nodes does not necessarily occur during every clock cycle. Hence, node switching activities are suppressed to a significant extent and consequently, energy dissipation is also reduced. One of the advantages of the 2PASCL circuit is that it can be made to behave like a static logic circuit.
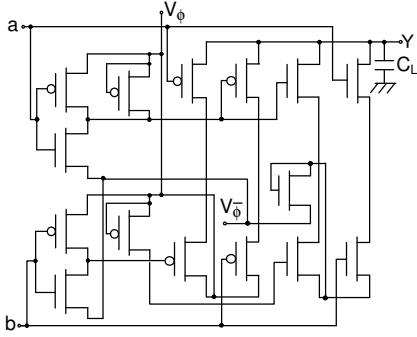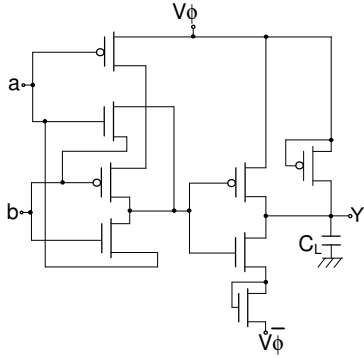
Fig. 4. Old 2PASCL 2XOR schematic.

Fig. 5. New design of 2PASCL 2XOR schematic.

IV. SIMULATION RESULTS

A. 2PASCL 2XOR comparison

Table II describes the details of the new 2PASCL 2XOR as compared to the previous design. Figure 4 shows the schematic of previous 2PASCL 2XOR logic circuit, where a and b are the inputs, V_ϕ and $V_{\overline{\phi}}$ are the the power supply clocks and Y is the output. A new 2PASCL 2XOR which has less transistors than the previous schematic is shown in Fig. 5. We derived the 2XOR CMOS presented by Wang et al. [21] to the new 2PASCL 2XOR by adding the nMOS and pMOS diodes only at the NOT logic of the original 2XOR. Then, split level sinusoidal power clocks are supplied as shown in Fig. 3. As in Table II, the number of transistors have been reduced from 15 to 8 in 2XOR. As MOSFETs in both 2PASCL and CMOS can be modeled as an ideal switch in series is included with a

TABLE II

DETAILS OF 2XOR LOGIC

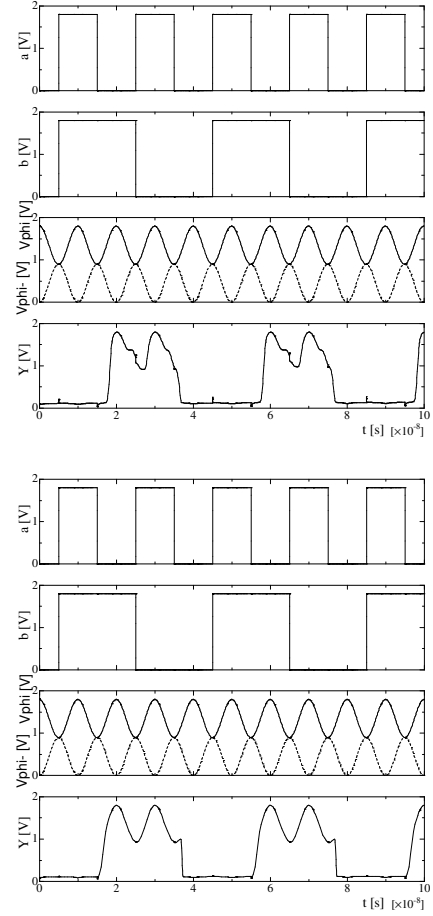|	Old 2PASCL 2XOR	New 2PASCL 2XOR
No. of transistors	15	8
W/L [μm]	0.6/0.18	0.6/0.18
W/L (nMOS diode) [μm]	40/40	40/40
V_ϕ, $V_{\overline{\phi}}$	0.9 V, 0.9 V	0.9 V, 0.9 V
C_L	0.01 pF	0.01 pF

Fig. 6. Output waveforms of (top) the old 2PASCL 2XOR and (bottom) the new 2PASCL 2XOR schematic.

resistor R in order to represent the sum of the effective channel resistance of the switch and the interconnect resistance. We reduced the total resistance by minimizing the number of transistors, consequently reducing the power dissipation.

In Fig. 6, we describe the simulation results of each schematic design. By comparing these two results at 50 MHz transition frequency, much better output waveforms generated by the schematic shown in Fig. 5 are observed. This is due to the shorter transmission path, consequently reduced signal degradation. Therefore, in the simulation, the power dissipated is calculated by integrating the product of voltage and current divided by the period of the primary input signal, T as follows:

$$P = \frac{1}{T} \int_0^T \left(\sum_{i=1}^n (V_{pi} \times I_{pi}) \right) dt, \qquad (15)$$

where V_p, the power supply voltage; I_p, the power supply current; and n, is the number of power supplies [8].

In Fig. 7, we compare the power dissipation of old and new design from 1 to 100 MHz transition frequencies. An average of half of the power dissipation can be saved by the new 2PASCL 2XOR design.
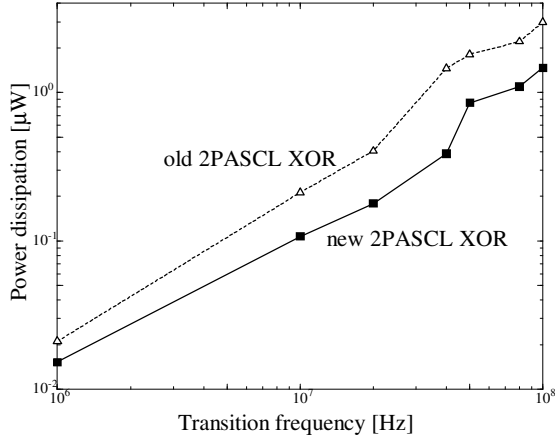
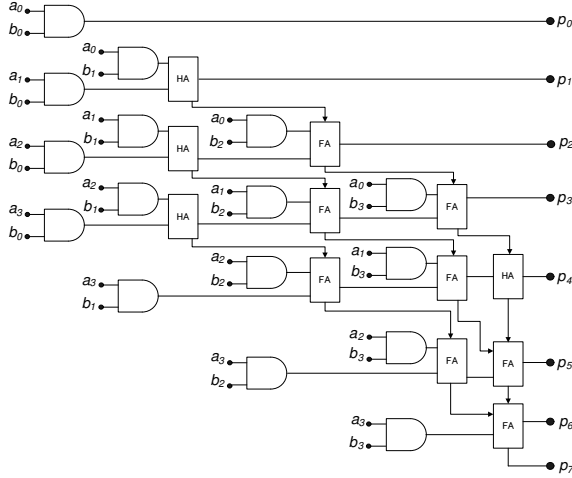Fig. 7. Power dissipation comparison of the old and new design of 2PASCL 2XOR.

Fig. 9. Output waveforms of 4×4-bit array 2PASCL multiplier at 10 MHz transition frequency from the simulation.

Fig. 8. Block diagram of 4×4-bit array multiplier.

Fig. 10. Power dissipation comparison of 4×4-bit array 2PASCL multiplier and 4×4-bit array CMOS multiplier.

B. 4×4-bit array 2PASCL multiplier

Figure 8 shows the diagram of 4×4-bit array multiplier which consists of sixteen ANDs, six full adders and four half adders logics. Load capacitance ranging from 0.01 to 0.1 pF are set at all outputs (p_0 to p_7). For fabrication, 2PASCL D-flipflops [17] are also used to capture all the 8-bit signals at the moment the clock is in HI state. In Fig. 9, we demonstrate the input and output waveforms of 10 MHz transition frequency 4×4-bit array 2PASCL multiplier. From these results, we confirm that our 4×4-bit array 2PASCL multiplier is functioning correctly. However, the signal glitch occurs at output p_2 to p_4. Figure 10 shows the power dissipation of 2PASCL multipliers which are about 55% less than CMOS multipliers of the same transistor size W/L of $0.6/0.18\mu$. However, from our simulation results, 4×4-bit array 2PASCL multiplier only shows a good logic functionality of up to 200 MHz transition frequency. We observe some signal degradations for transition frequency of more than 200 MHz. This is due to the charging time T which is 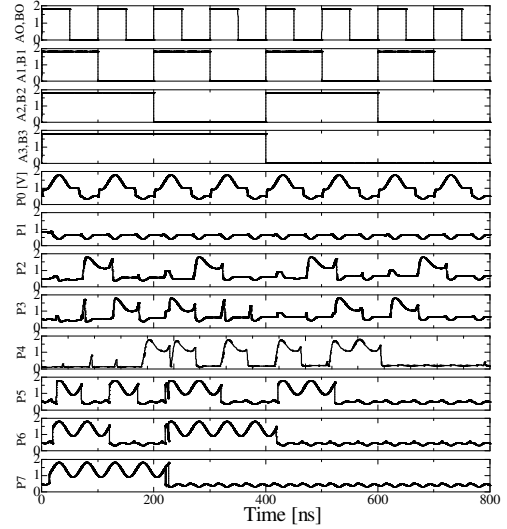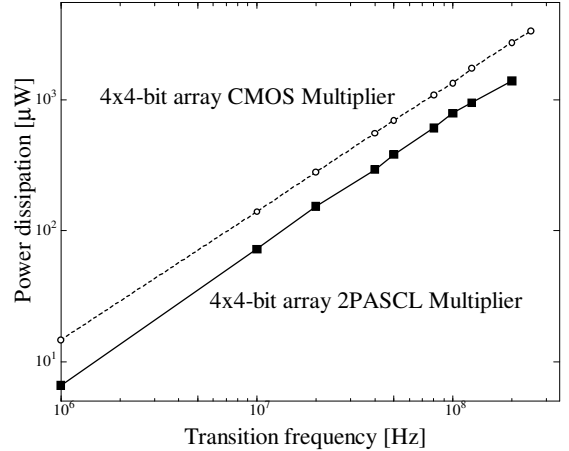much slower than conventional CMOS. T is also proportional to RC_L i.e. the longer the path, the larger T is needed. These input frequencies are adequate for the applications mentioned in Section I.

V. CONCLUSION

In this paper we designed and simulated a 4×4-bit array two-phase clocked adiabatic CMOS logic (2PASCL) multiplier circuit using a new 2XOR. The simulation results show that power consumption in the 2PASCL multiplier is considerably less than that in a CMOS. For instance, when the input frequency is simulated from 1 to 100 MHz, the 2PASCL multiplier logic dissipates minimally as only half of the power dissipated by a static CMOS logic circuit. We believe that the proposed adiabatic logic circuit is advantageous for ultra low-energy computing applications. As for our future work, we will further evaluate the cause of the signal glitches in 2PASCL.

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