Memristor 1T-SRAM with Adiabatic Driving

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***Abstract*—This paper proposes a novel adiabatic static random access memory (SRAM) using memristor. The proposed SRAM which is a sinusoidal driving consists of one NMOS transistor and one memristor (i.e. 1T1M type). The proposed SRAM also is driven by an optimal voltage resulting in a decrease of energy dissipation. From SPICE simulation results, we show that the energy dissipation of proposed 1T1M-SRAM with a sinusoidal driving voltage is lower than that of the conventional pseudo-SRAM called 1T1C, and the proposed circuit is especially effective against reducing power consumption at logic Hi-state.**

***Keywords*—SRAM, pseudo SRAM, memristor, adiabatic, low power**

I. Introduction

In 1971, Chua has pointed out the existence of the fourth passive component called memristor [1]. This element is defined by a nonlinear relationship between the charge and the magnetic flux, and therefore it can be used as a nonlinear resistor with memory. After 37 years, the first experimental realization of memristor has demonstrated in a solid-state thin film two terminal device by HP Labs [2]. The memristive effect has achieved by moving the doping front along the device. This discovery has attracted a great attention. Many potential applications are reported, e.g., the memories for low cost technology [3], [4], programmable logic [5], and reconfigurable logic [6].

The adiabatic logics [7]– [15] and the adiabatic memories [16]– [21] are a very attractive solution for low power consumption but the papers have proposed that the conventional memory structures have used – e.g. 6 transistor (6T) based, 8T, inverted-latch, and Flip-Flops (FF), and whereby there is positive need for small-size and low-power adiabatic memory for the next-generation.

In this paper, we present a new adiabatic pseudo-SRAM using a memristor. The proposed SRAM builds on a single NMOS transistor and one memristor, and hence it is like DRAM. The proposed SRAM also is driven by an optimal sinusoidal voltage resulting in a decrease of energy dissipation. The rest of the paper is organized as follows. Section II summarizes the most important properties of the adiabatic logic. The properties of memristor is briefly described in Section III. The proposed memristor based 1T-SRAM is presented and is evaluated in Section IV. Finally the conclusions are given in Section V.

II. Adiabatic Logic

A. Conventional vis-a-vis Adiabatic Switching

Te conventional switching can be understood by using a simple CMOS inverter. The CMOS inverter can be considered to consist of a pull-up and pull-down networks connected to a load (or internal) capacitance C. The pull-up and pull-down networks are actually MOS transistors in series with the same load C. Both transistors can be modeled by an ideal switch in series with a resistor which is equal to the corresponding channel resistance of the transistor in the saturation mode, as shown in Fig. 1(a). When the logic level in the system is "1", there is a sudden flow current through R, where R is equivalent resistance of PMOS pull-up network. A charge $Q = CV_{dd}$ is delivered to the load and the energy which the supply applies is $E_s = QV_{dd} = CV_{dd}{}^2$, where V_{dd} is a DC power supply voltage. The energy stored into the load C is a half of the supplied energy:

$$E_{stored} = \frac{1}{2}CV_{dd}{}^2. \tag{1}$$

The same amount of energy is dissipated during the discharge process in the NMOS pull-down network because no energy can enter the ground rail $Q \times V_{gnd} = Q \times 0 = 0$. From the energy conservation law, a conventional CMOS logic emits heat and, in this way, it wastes energy in every charge-discharge cycle:

$$\begin{aligned} E_{total} &= E_{charge} + E_{discharge} \\ &= \frac{1}{2}CV_{dd}{}^2 + \frac{1}{2}CV_{dd}{}^2 \\ &= CV_{dd}{}^2. \end{aligned} \tag{2}$$

If the logic is driven by a certain frequency f $(= 1/T)$, where T is the period of the signal, then the power of the CMOS gate is determined as:

$$P_{total} = \frac{E_{total}}{T} = CV_{dd}{}^2 f. \tag{3}$$

Adiabatic switching is commonly used to minimize energy loss during charging/discharging. The word "adiabatic" (Greek

adiabatos, which means impassable) indicates a state change that occurs without heat loss or gain. During adiabatic switching, all the nodes are charged or discharged at a constant current in order to minimize power dissipation. This is accomplished by using AC power supplies to initially charge the circuit during specific adiabatic phases and then discharge the circuit to recover the supplied charge. The principle of adiabatic switching can be best explained by contrasting it with the conventional dissipative switching technique. The main idea in the adiabatic switching shown in Fig. 1(b) is that transitions are considered to be sufficiently slow so that heat is not emitted significantly. This is made possible by replacing the DC power supply by a resonance LC driver, an oscillator, a clock generator, etc. If a constant current source delivers the $Q = CV_{dd}$ charge during the time period ΔT, the energy dissipation in the channel resistance R is given by

$$\begin{aligned} E_{diss} &= \xi P \Delta T \\ &= \xi \overline{I}^2 R \Delta T \\ &= \xi \left(\frac{CV_{dd}}{\Delta T} \right)^2 R \Delta T, \end{aligned} \tag{4}$$

where $\overline{I}$ is considered as the average of the current flowing to C, and ξ is a shape factor which depends on the shape of the clock edges [22]. It takes on the minimum value $\xi_{min} = 1$ if the charge of the load capacitor is DC modulated. For a sinusoidal current, $\xi = \pi^2/8 = 1.23$. The above equation indicates that when the charging period ΔT is indefinitely long, in theory, the energy dissipation is reduced to zero. This is called an adiabatic switching [7].

III. Memristor

A. Theory

In [1], a charge-controlled memristor as shown in Fig. 2 is defined as a two-terminal element in which the magnetic flux φ between the terminals is a function of the amount of electric charge q. The voltage $v(t)$ across the memristor is given by

$$v(t) = M(q(t))i(t) \tag{5}$$

where $M\left(q(t)\right) = d\varphi\left(q(t)\right)/dq(t)$ is a *memristance*. The memristance becomes constant which acts like resistance while in the linear case. However, $\varphi - q$ relation is non-linear whereby the element is referred to as memristance which can be charge-controlled.

B. SPICE model of HP's memristor

In [2] the authors have realized a memristor which consists of a thin layer of TiO_2 and a second oxygen deficient layer of TiO_{2-x} sandwiched between two Pt nanowires. The voltage-current relationship of this memristor is modeled as:

$$M\left(q(t)\right) = \left[R_{\mathrm{ON}} \frac{w(t)}{L} + R_{\mathrm{OFF}} \left(1 - \frac{w(t)}{L} \right) \right] i(t), \tag{6}$$

where R_{ON} is the resistance for completely doped memristor, R_{OFF} is the resistance for the undoped region and also L is the TiO_2 film thickness. The width of the doped region $w(t)$ is given by

$$\frac{dx(t)}{dt} = \mu_v \frac{R_{\mathrm{ON}}}{L^2} i(t), \tag{7}$$

where μ_v represents the average dopant mobility.

Lehtonen and Laiho have solved the differential equation (7) by using injective function [23] and obtained SPICE model of HP's memristor. Using their SPICE parameters memristance function is calculated as following:

$$M\left(q(t)\right) = \frac{d\varphi\left(q(t)\right)}{dq(t)} = 25 \left[1 - \left(2q(t) - 1 \right)^2 \right]. \tag{8}$$

Figure 3 shows the voltage-current relationship (I-V curve) of HP's memristor when above condition is provided. In this work, SPICE model of memristor is used as shown in this figure.

IV. Proposed 1T-SRAM

A. Structure

Figure 4 is the basic structure for a memristor NMOS storage cell [4]. This storage cell is a similar 1T1C circuit using FRAM [24] or capacitor [25]. Figure 5 depicts timing diagram for writing "1" and "0" operation which has described in [4]. For writing a logic "1," the memristor receives a positive bias to maintain an ON state. This is equal to the memristor being programmed as a logic HI. To program a "0" a reverse bias is applied to the memristor, which makes the memristor resistance high. This is comparable to logic LOW being programmed.

The proposed 1T-SRAM structure is the same as memristor NMOS storage. However, timing diagram is clearly distinct in that the threshold voltage of NMOS transistor is considered. Figure 6(a) illustrates the proposed timing diagram in order to achieve optimum output signal and low-power dissipation. The on-state voltage drop of the NMOS causes decreasing output voltage (V_{out}), hence the voltage for driving signal (DS) should set as: $\geq V_{dd} + V_t$, where V_{dd} and V_t are power supply voltage and threshold voltage for NMOS resistor, respectively. As a result voltage bias level (VL) is set to $\geq (V_{dd} + V_t)/2$. To reduce the power consumption of memory, top level for writing signal (WS) is adjusted to V_{dd} because switching losses increase when the gate voltage is driven beyond V_{dd}. When the proposed SRAM is changed to adiabatic mode, DS waveform is replaced pulse by trapezoidal (or sinusoidal) as shown in Fig. 6(b).

B. Comparison and Evaluation

To evaluate the operation and the energy dissipation of memory, the 1T-based adiabatic SRAM was tested by SPICE simulation using an 0.18 μm, 1.8 V CMOS standard process technology. The transistor size W/L is 0.6 μm/0.18 μm for the NMOS transistor.

The SPICE simulation results obtained for the 1T-SRAM are shown in Fig. 7. Figure 7(a) demonstrates the input signals: pulse, trapezoidal and sinusoidal, the write-bit signal: WS; Figure 7(b) shows the output waveform. From these figure

the output data is correctly hold-state after writing "1" and "0."

Table I summarizes the energy dissipation values of each function. As can be seen from this table, the energy dissipation of proposed 1T-SRAM with sinusoidal wave is much smaller than that of 1T-SRAM with conventional pulse driving.

Figure 8 shows the comparison of energy dissipation between proposed (1T1M) SRAM and conventional (1T1C). The capacitor size of 1T1C is set to 100 fF, if the capacitor is fabricated using poly insulator poly (PIP). This figure shows that energy dissipation of 1T1M is drastically decreased compared to the 1T1C, especially at "1" writing mode.

V. Conclusion

In this paper we have presented a new adiabatic memory which is consists of 1T1M. The simulation results have shown that 1T1M driving sinusoidal wave has 17.5 fJ when each "1" and "0" write, and also the energy dissipation of proposed memory is smaller than that of conventional 1T1C memory cell.

References

[1] L. O. Chua, "Memristor–The missing circuit element," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 5, pp. 507–519, Sep. 1971.

[2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature,* vol. 453, pp. 80–83, May 2008.

[3] Y. Ho, G. M. Huang, and P. Li, "Nonvolatile memristor memory: Device characteristics and design implications," in *Proc. IEEE Int. Conf. Computer Aided Design* (ICCAD 2009), San Jose, CA, Nov. 2–5, 2009, pp. 485–490.

[4] K. Eshraghian, K. -R. Cho, O. Kavehei, S. -K. Kang, D. Abbott, and S. -M. S. Kang, "Memristor MOS content addressable memory (MCAM): Hybrid architecture for future high performance search engines," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, in press.

[5] J. Rajendran, H. Manem, R. Karri, and G. S. Rose, "Memristor based programmable threshold logic array," in *Proc. IEEE int. Symp. Nanoscale Architectures* (NANOARCH 2010), Anaheim, CA, June 17-18, 2010, pp. 5–10.

[6] Q. Xia, W. Robinett, M. W. Cumbie, N. Banerjee, T. J. Cardinali, J. J. Yang, W. Wu, X. Li, W. M. Tong, D. B. Strukov, G. S. Snider, G. Medeiros-Ribeiro, and R. S. Williams, "Memristor-CMOS hybrid integrated circuits for reconfigurable logic," *Nano Lett.*, vol. 9, no. 10, pp. 3640–3645, Oct. 2009.

[7] L. J. Svensson, and J. G. Koller, "Adiabatic charging without inductors," in *Proc. IEEE Int. Workshop Low Power Design* (IWLPD '94), Napa Valley, CA, Apr. 22–27, 1994, pp. 159–164.

[8] A. G. Dickinson and J. S. Dencker, "Adiabatic dynamic logic," *IEEE J. Solid-State Circuits*., vol. 30, no. 3, pp. 311–315, Apr. 1995.

[9] Y. Moon, D. K. Jeong, "An efficient charge recovery logic circuit," *IEEE J. Solid-State Circuits*., vol. 31, no. 4, pp. 514–522, Apr. 1996.

[10] S. Kim and M. C. Papaefthymiou, "True single-phase energy-recovering logic for low-power, high-speed VLSI," in *Proc. IEEE Int. Symp. Low-Power Electronics and Design* (ISLPED '98), Monterey, CA, Aug. 10–12, 1998, pp. 167–172.

[11] D. Maksimović, V. G. Oklobdžija, B. Nikolić, and K. W. Current, "Clocked CMOS adiabatic logic with integrated single-phase power-clock supply," *IEEE Trans. VLSI Syst*., vol. 8, no. 4, pp. 460–463, Aug. 1998.

[12] Y. Ye and K. Roy, "QSERL: Quasi-static energy recovery logic," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, pp. 239–248, Feb. 2001.

[13] S. Nakata, "Adiabatic charging reversible logic using a switched capacitor regenerator," *IEICE Trans. Electron*., vol. E87-C, no. 11, pp. 1837–1846, Nov. 2004.

[14] Y. Takahashi, T. Sekine, and M. Yokoyama, "VLSI implementation of a 4×4-bit multiplier in a two phase drive adiabatic dynamic CMOS logic," *IEICE Trans. Electron*., vol. E90-C, no. 10, pp. 2002–2006, Oct. 2007.

[15] N. Anuar, Y. Takahashi, and T. Sekine, "Two phase clocked adiabatic static CMOS logic and its logic family," *IEEK J. Semiconductor Technology and Science*, vol. 10 no. 1, pp. 1–10, Mar. 2010.

[16] D. Somasekhar, Y. Yibin, and K. Roy, "An energy recovery static RAM memory core," in *Proc. IEEE Symp. Low Power Electronics*, Oct. 9–11, 1995, p. 62.

[17] J. Kim, C. H. Ziesler, and M. C. Papaefthymiou, "Energy recovering static memory," in *Proc. ISLPED 2002*, Monterey, CA, Aug. 12–14, 2002, pp. 92–97.

[18] S. Zhang, J. Hu, and D. Zhou, "A low-power adiabatic content-addressable memory," in *Proc. IEEE Midwest Symp. Circuits and Syst.* (MWSCAS 2007), Montreal, Canada, Aug. 5–8, 2007, pp. 1548–3746.

[19] R. Karakiewicz, R. R. Genov, and G. Cauwenberghs, "480-GMACS/mW resonant adiabatic mixed-signal processor array for charge-based pattern recognition," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2573–2584, Nov. 2007.

[20] S. Nakata, T. Kusumoto, M. Miyama, and Y. Matsuda,; "Adiabatic SRAM with a large margin of VT variation by controlling the cell-power-line and word-line voltage," in *Proc. IEEE Int. Symp. Circuits and Syst.* (ISCAS 2009), Taipei, Taiwan, May 24–27, 2009, pp. 393–396.

[21] J. Chen, D. Vasudevan, E. Popovici, M. Schellekenst, and P. Gillen, "Design and analysis of a novel 8T SRAM cell for adiabatic and non-adiabatic operations," in *Proc. IEEE Int. Conf. Electro., Circuits, and Syst.* (ICECS 2010), Athens, Greek, Dec. 12–15, 2010, pp. 434–437.

[22] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," *Nature Nanotechnology*, vol. 3, pp. 429–433, 2008.

[23] E. Lehtonen, and M. Laiho, "CNN using memristors for neighborhood connections," in *Proc. IEEE Int. Workshop Networks and Their App.* (CNNA 2010), Berkeley, CA, Feb. 3–5, 2010, 4pages.

[24] R. Ogiwara, S. Tanaka, Y. Itoh, T. Miyakawa, Y. Takeuchi, S. M. Doumae, H. Takenaka, I. Kunishima, S. Shuto, O. Hidaka, and S. Ohtsuki, "A 0.5-μm, 3-V 1T1C, 1-Mbit FRAM with a variable reference bit-line voltage scheme using a fatigue-free reference capacitor," in *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 545–551, Apr. 2000.

[25] W. Leung, F. -C. Hsu, M. -E. Jones, "The ideal SoC memory: 1T-SRAM ™," in *Proc. IEEE Int. ASIC/SOC Conf.*, Arlington, VA, Sep. 13–16, 2000, pp. 32–36.

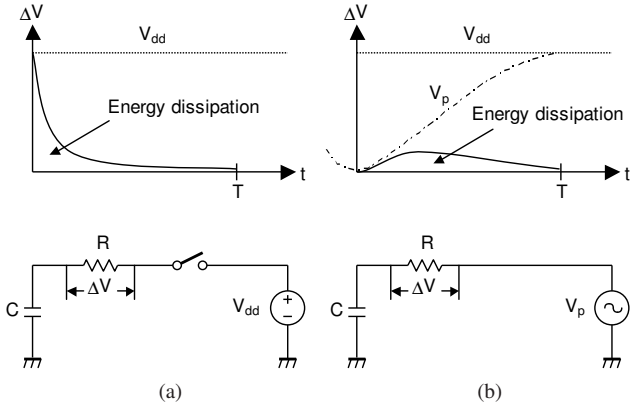


Fig. 1. RC tree model. (a) CMOS Charging. (b) Adiabatic Charging.

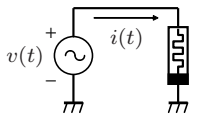


Fig. 2. Memristor.

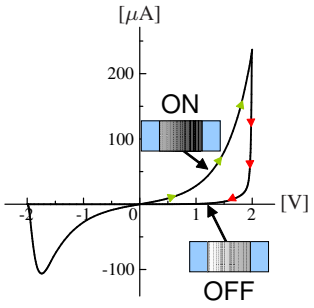


Fig. 3. I-V curve of HP's memristor.

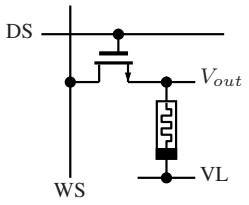


Fig. 4. Memristor-NMOS storage cell.

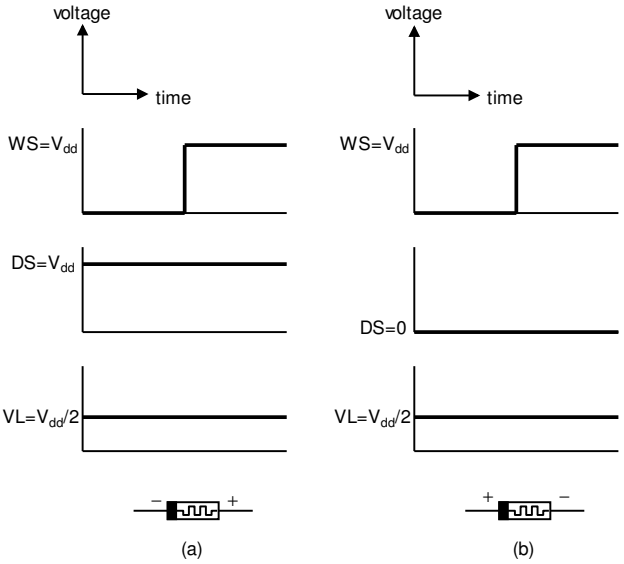


Fig. 5. Timing diagram of memristor-NMOS storage cell. (a) Program "LOW" resistance "1." (b) Program "HI" resistance "0."

TABLE I
COMPARISON OF ENERGY DISSIPATION DEPEND ON THE DIFFERENCE IN INPUT WAVEFORM

Waveform	Energy dissipation [fJ]
Pulse	34.3 (100%)
Trapezoidal	33.3 (97%)
Sinusoidal	17.5 (51%)

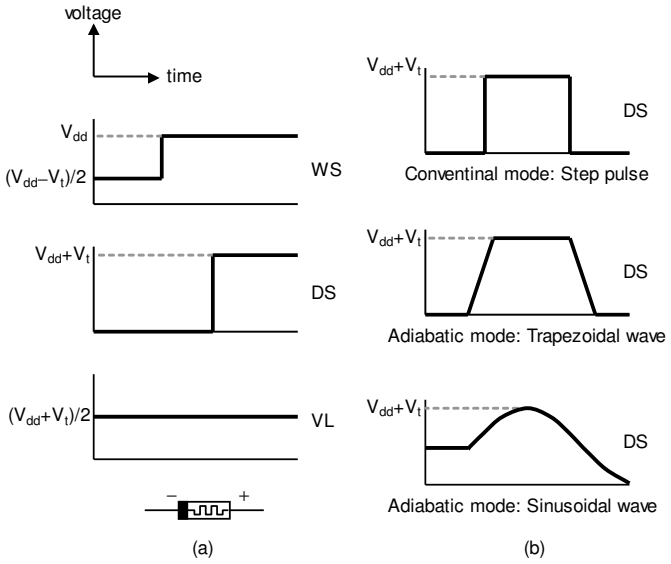
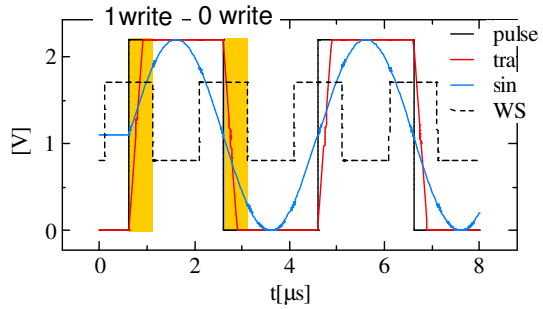
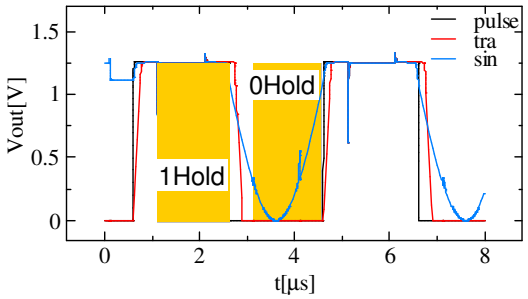


Fig. 6. Proposed timing diagram. (a) D/S, WS and VL with optimal voltage. (b) adiabatic mode.



(a) Voltage timing: WS and DS (pulse, tra. and sin. wave).



(b) Output waveform.

Fig. 7. Input/output waveforms of 1T-SRAM using memristor.

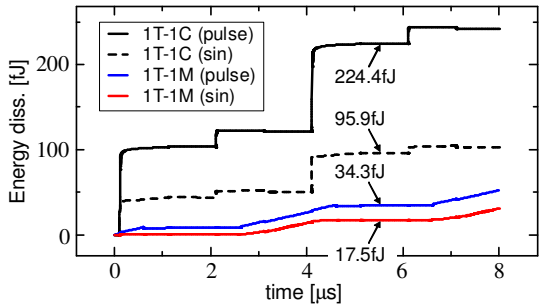


Fig. 8. Comparison of energy dissipation between proposed 1T1M-SRAM and conventional 1T1C.