FPGA Design and Implementation of Electrocardiogram Biomedical Embedded System

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***Abstract*— This paper presents a FPGA design and implementation of Electrocardiogram (ECG) biomedical embedded system (ECG-SoC). It performs ECG pre-processing and heart rate variability (HRV) feature extraction which suitable for remote homecare monitoring and rural health care application. The ECG-SoC is designed using hardware/software co-design technique based on offline dataset from MIT-BIH database. Altera Cyclone II DE2-115 FPGA platform was used for system prototyping and functionality verification. The computation results are displayed on Nios II-Linux terminal and produce output files for post analysis executed on the host personal computer (PC).**

I. Introduction

According to the statistic reported by the World Health Organization (WHO) in 2012, cardiovascular disease account the largest proportion of deaths about 48% [1]. It is estimated that 7.3 million were due to coronary heart disease and 6.2 million are stroke problems. In fact, heart disease accounts for one out of every three deaths, and this percentage is increasing in every year [2].

Human heart activity can be electrically recorded in the form of an electrocardiogram (ECG) signal using a non-invasive tool [3]. An ECG can readily reveal a number of heart malfunctions or disorders, such as cardiovascular disease (CVD), stroke and sudden cardiac arrest. Thus, the main challenge of an ECG device arises from the computational demand for processing huge amounts of large scale ECG data analysis in parallel. Also, in the real-time computation under stringent time constraints, and transmission of huge amounts data over a communication link to a large set of computing devices to another location under life critical conditions. There are also cases in homecare and emergency where the patient is mobile and remotely monitored. Therefore, a portable ECG monitoring device with improved accuracy and integrates more functionality to fit in homecare services with acceptable performance is desired. Portable in size and mobility features will contribute in heart monitoring become easier. The highly accurate portable ECG is necessary because a misinterpretation for heart disease signal may cause fatal.

Previous work on the ECG analysis can be categorized into four kinds of solutions: (i) classical stationary machine solutions, (ii) SoC solutions [4], (iii) handheld device solutions [5], and (iv) ASIC solutions [6]. The classical solutions do not allow patient mobility nor remote analyses since the devices were plugged, it requires an excessive amount of beds in a healthcare center. The SoC solution runs 12-lead analyses in a single chip to provide reliable ECG analysis. The commercial solution [7] takes eighth input sensor lines, calculates lead signals, and analyze them in one digital signal processing (DSP) step, but this process is time consuming. A new solution [8] uses a flexible SoC that combines the acquisition of multiple biomedical signals, such as ECG, electroencephalography (EEG), and respiration signals, with on-chip digital signal processing. Whereas handheld solutions [9] only read and transmit data, this novel solution uses a portable Linux based ECG measurement and monitoring system that supports 12-lead ECG data acquisition and remote diagnosis via the internet. The ASIC solution [10] is only used for data acquisition before transmission.

In order to integrate HRV analysis function on an ECG device, one recommended method is to design the device using System-on-Chip (SoC) technology to produce a portable heart monitoring device which suitable for home care. This paper presents a SoC based on the ECG biomedical embedded system (ECG-SoC) using hardware/software co-design technique and Altera technology to perform ECG pre-processing and HRV feature extraction based on MIT-BIH offline database [11].

The paper is organized as follows. Sections II presents the system functionality whereas Section III presents the propose system architecture and design in methodology. The result is presented in Section IV. While the conclusion and the recommendation for future enhancement are discussed in Section V.

II. ECG-SoC System Functionality

In the preprocessing stage, the Pan and Tompkins algorithm is adapted from [12] to detect QRS complex of ECG data in order to perform HRV analysis. This detection module

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consists of an Infinite Impulse Response (IIR) filter with band pass filter frequency of 5 Hz to 15 Hz.

Fig. 1 shows the flow process of the ECG signal pre-processing and HRV feature extraction. He filtered output is differentiated to provide complex slope information for peak detection. The squaring function is replaced by the absolute function to speed up the computation by toggling all negative peaks that possible to generate positive values. The moving window integration is applied to smooth out the data.

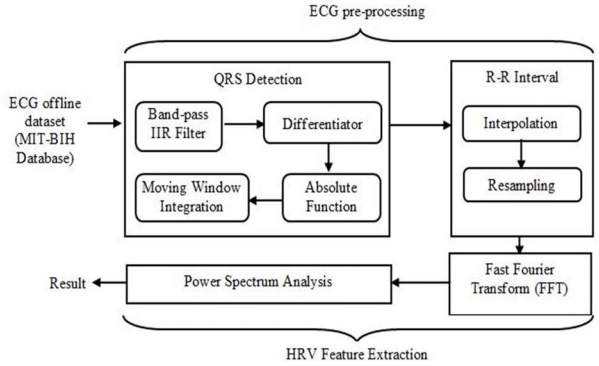

Figure 1. Block diagram of ECG pre-processing and HRV feature extraction.

After QRS complex detection, the ECG signal is transformed into the valley-like signal which has two peaks with significant different height. To detect heartbeat from ECG signal, the R peaks of QRS complex are used. In the R-R interval module, the peak of the ECG signal is detected by comparing the current value with next eight values. The larger values than the next eight values and greater than a set threshold level are treated as the R peak values of ECG [13]. In the next block unit, the interpolation is done between two R-R intervals to obtain a continuous R-R intervals result from the calculation of the detected peaks. The reciprocal of the R-R interval is heart rate value in Hertz (s^{-1}). However, common unit for heart rate is min^{-1}. To gain the heart rate value in min-1, multiply the reciprocal of the R-R interval by 60.

The continuous heart rate is then resampled at 4 Hz. Then, Fast Fourier Transform (FFT) is applied to the resampled signal to get the power spectrum of the R-R interval data. The FFT is performed for both real and imaginary parts. All the values were essential for power spectral analysis according to (1).

$$PS = \frac{\sqrt{r^2 + i^2}}{N} \tag{1}$$

where r is represented for real part, i is imaginary part and of N is the total number of R-R interval data or Heart Rate (HR) data being FFT.

Meanwhile, to obtain the heart rate variability (HRV) of the HF band, and integration of the power spectrum is performed from 0.15 Hz to 0.4 Hz. The following (2), (3) and (4) are applied.

$$HRV_{VLF} = \sum_{f=0.008}^{0.04} \frac{|HR(f)|^2}{T} \tag{2}$$

$$HRV_{LF} = \sum_{f=0.04}^{0.15} \frac{|HR(f)|^2}{T} \tag{3}$$

$$HRV_{HF} = \sum_{f=0.15}^{0.4} \frac{|HR(f)|^2}{T} \tag{4}$$

where *HR (f)* is the frequency spectrum of the heart rate and *T* is time. Based on the spectral diagram of the heart rate, there are three types of power bands that can be derived from different bands of frequencies. These power bands are very low frequency (*VLF*: 0.008 Hz to 0.04 Hz), low frequency (*LF*: 0.04 Hz to 0.15 Hz), and high frequency (*HF*: 0.15 Hz to 0.4 Hz).

III. METHOD

ECG-SoC architecture consists of both hardware and software partitions, which require hardware/software (HW/SW) co-design techniques. It incorporates general purpose microprocessor to execute application software and device driver as software partition and acts as the main controller to instruct the other system peripherals. It also utilizes Altera Nios II processor, Avalon on-chip communication fabric and the Nios II-Linux as an embedded operating system. The ECG-SoC system architecture design which targeted to Altera Cyclone II FPGA technology is shown in Fig.2.

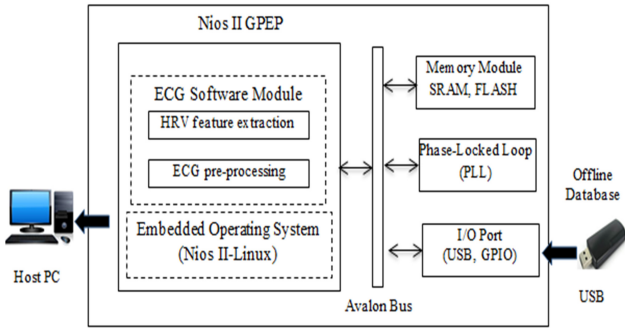

Figure 2. ECG-SoC Cyclone II FPGA.

The hardware partition consists of on chip memory or external memory controllers, phase-locked loop and I/O controllers. The memory modules store the image of embedded operation system which consists of program, MIT-BIH offline database, and other important files, as well as temporary storage during application execution. The phase-locked loop controls the system clock signal and running frequency. While, the I/O controller communicates and transmit the data external to the outside world. Among all these peripherals, there is a system bus which provides a communication channel according to Avalon bus switch fabric protocol.

Fig.3 shows the design methodology of the ECG-SoC. It consists of four phases, which are system hardware architecture design, Nios II-Linux embedded operating system (OS) development, ECG biomedical signal processing application with software configuration and system integration. The detail of each phase will be discussed in the next subsections. During the design process, several EDA tools are required, such as QUARTUS II, SOPC Builder, Nios II IDE and Nios II-Linux cross compiler.

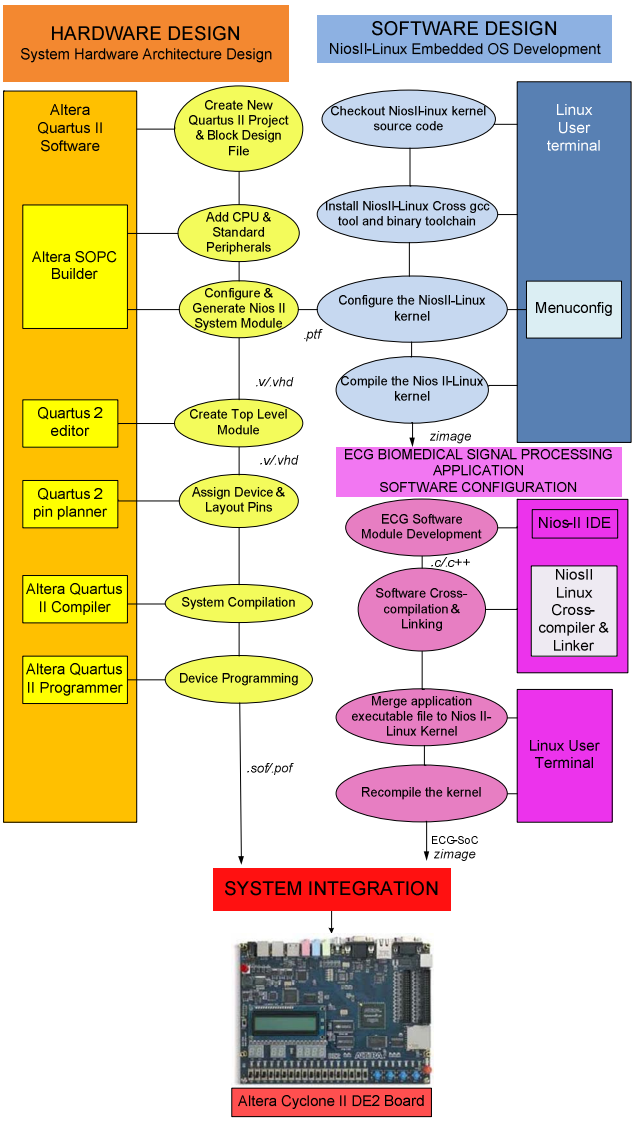

Figure 3. ECG-SoC design methodology.

A. System Hardware Architecture Design

For the first phase, the general purpose Nios II CPU, memory and other standard peripherals are defined to form a standard Nios II system module using SOPC Builder. The configuration involved the reset vector and exception vector of the Nios II processor, the base address and interrupt priority (IRQ) assignment of every peripherals, as well as their clock signal sources. The SOPC builder generation process generates multiple Verilog HDL (.v) files and the system configuration file (.ptf) which later is going to be used in configuring and compiling the software module, as well as Nios II-Linux kernel. After the SOPC Builder generation process, Altera Quartus II takes over to create a top level system architecture of the Nios II system module and pin assignment is made. This also includes the system setting such as the targeted development board, devices and pin options, synthesis, fitting and timing analysis process to generate the netlist and hardware programming file (.sof/.pof) which is ready to be downloaded into Altera FPGA development board in final system integration. While the hardware part was fully configured, it generates multiple HDL files of the system peripherals in Verilog (.v), and the system configuration file (.ptf).

B. Nios II-Linux Embedded Operating System Development

Nios II-Linux is a terminal based Linux embedded operating system, which it can run and compile Linux based programs and libraries. To compile the Nios II-Linux kernel of ECG-SoC, the system configuration files (.ptf) of the targeted hardware system generated by SOPC Builder is required to configure and compiling the Linux kernel. Select the target processor to execute the Linux kernel as well as a memory module to load the kernel image. Moreover, the Linux kernel, peripheral device kernel library also needs to be identified and installed.

C. ECG Biomedical Signal Processing Application with Software Configuration

This task requires the embedded software development of the ECG biomedical signal processing modules, such as ECG signal pre-processing and HRV feature extraction based on the well established algorithm as described in Section II. The embedded software also generates output data files which later executed by a host PC for graph plotting for post analysis. Since Nios II-Linux is an embedded OS with the target processor set to Altera Nios II CPU, the ECG biomedical signal processing application software program must be cross compiled before it is executed by the Nios II processor. This task can be done by using the binary tool chain and libraries. In addition to that, any cross compiled C/C++ executable program that is written for Nios II-Linux must be included inside Nios II-Linux zImage file. The kernel is then recompiled again to produce a new zImage file and ready to be downloaded into the Altera FPGA development board.

D. System Integration

In the final system integration, the hardware programming file (.sof) and the updated Nios II-Linux zImage file is both downloaded into Altera Cyclone II DE2-115 platform for system functionality verification and perform the evaluation.

IV. Results And Discussions

Table I contains descriptions of the ECG system specification. This paper used 200 Hz, sampling frequency for the ECG signals and threshold values is 8000 Hz. Meanwhile, to reduce the dimensionality of heart rate data, 4 Hz the resampling frequency has been chosen. The 120 000 is the offline ECG data come out of the MIT-BIH database which store in pendrive in text file format. With the larger ECG dataset will make the processing become more accurate.

TABLE I. ECG SYSTEM SPECIFICATION

Specifications	Values
Sampling frequency	200 Hz
Threshold value	8000 Hz
Resampling frequency	4 Hz
Total ECG data	120 000
FFT count	1024

This subsection generates results from ECG pre-processing and HRV feature extraction software. The results are obtained after the compilation of the ECG software, including QRS detection demonstrating a differentiated and smoothed output, the peaks detected for R-R interval block, interpolation and resampling outputs, and FFT outputs. These FFT outputs consist of both real and imaginary parts. Fig. 4 shows the output graph plotted using Matlab software which represents the slope of the ECG signal.

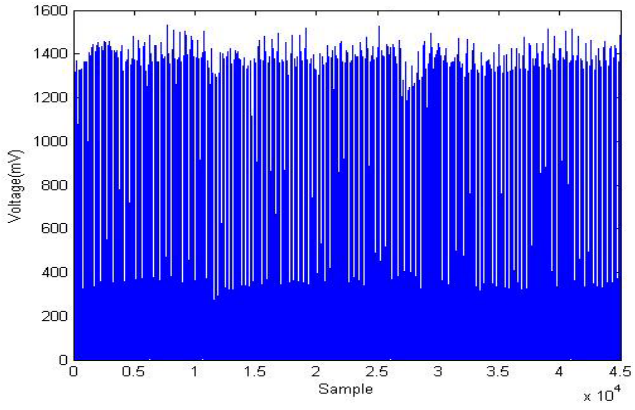

Figure 4. Differentiated signal.

Noted that each data is converted to its absolute value to cover all negative peaks of ECG signals. Fig. 5 shows the values are greater than in Fig. 4 which is performed right before the smoothing operation by moving window integration.

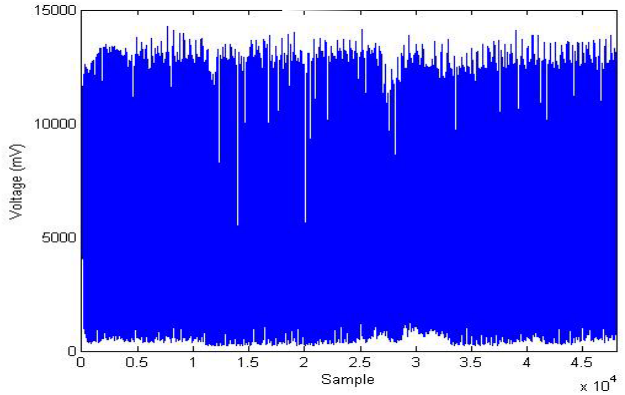

Figure 5. Smoothed signal.

The peaks are detected in the R-R intervals as shown in Fig. 6 for the interpolation. While, the resampling of ECG signals after interpolation was illustrated in Fig. 7.

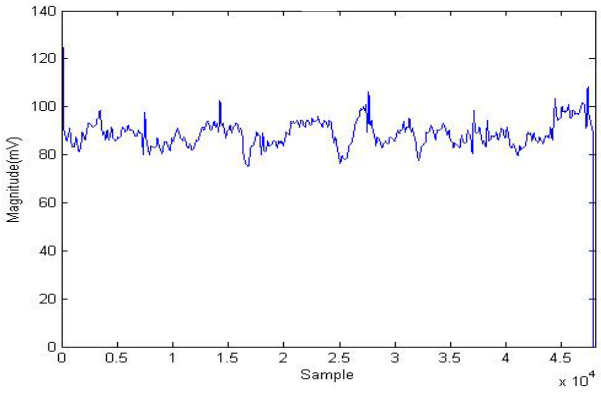

Figure 6. Interpolation.

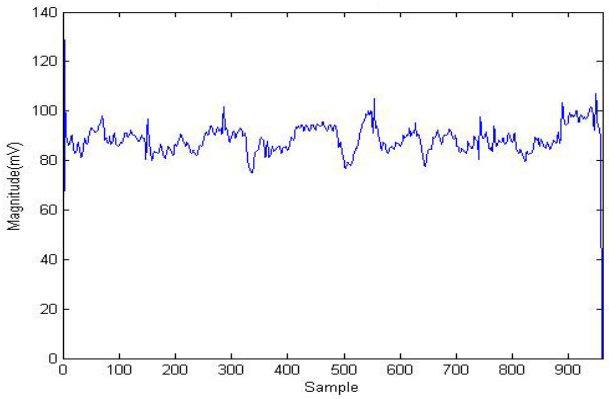

Figure 7. Resampling.

Fig. 8 depicted the FFT output to identify the peaks in the ECG signal. Thus, noise can be removed from ECG signal.

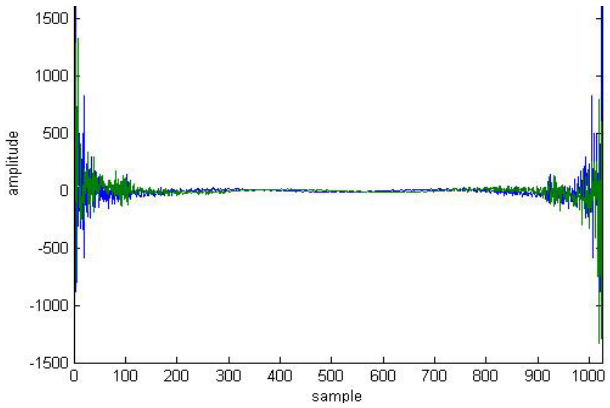

Figure 8. FFT output.

The result of power spectrum analysis that ranged up to frequency 1 Hz is shown in Fig. 9. The graph is marked with dotted lines to show the frequency range of VLF as the

maximum range with the red lines, LF as the maximum limit with the black lines, and HF as the limiting with the yellow lines, respectively. For the normal case ECG data, the highest frequency shows an amplitude within a small value. The frequency that contain of the ECG signal can be identified directly from the frequency sample value that is corresponding with the peak value.

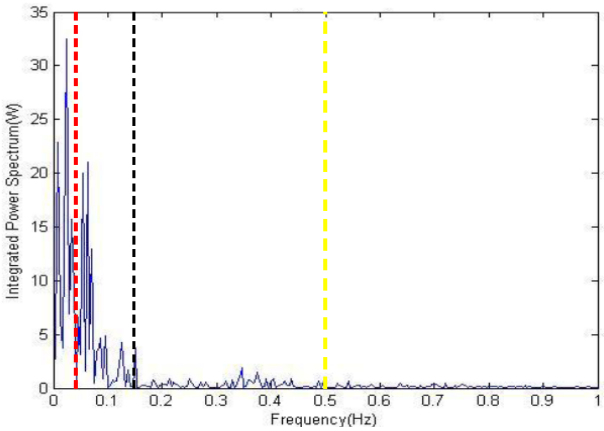

Figure 9. Integrated power spectrum versus frequency.

V. CONCLUSION

This paper has presented a SoC based ECG biomedical embedded system (ECG-SoC) design using hardware/software co-design techniques and Altera technology to perform ECG pre-processing and HRV feature extraction based on offline dataset. The main limitation of this system is the time consuming embedded software execution causes the system performance bottleneck. In addition, it still depends on the host PC to perform the frequency domain feature extraction and graph plotting. For the feature recommendation, the hardware accelerator is desired to boost up the computation performance, as well as carry out the on-chip feature extraction in the frequency domain. Besides that, the signal acquisition unit is designed for online monitoring and integrates state-of-the-art algorithm for heart disease detection as a decision support system.

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