4-bit Ripple Carry Adder of Two-Phase clocked Adiabatic Static CMOS Logic: a comparison with static CMOS

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***Abstract*—The paper presents a new quasi energy recovery logic family that uses two complementary split-level sinusoidal power supply clock for digital low power applications such as sensors. The proposed two-phase adiabatic static CMOS logic circuit (2PASCL) is using the principle of energy recovery and adiabatic switching. It has switching activity that is lower than dynamic logic and can be directly derived from static CMOS circuits. We have designed and simulated a 4-bit ripple carry adder (RCA) using 2PASCL logic gates implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the gates. From the simulation result, it shows that 2PASCL can save an average of 71.3% of energy dissipation compared with static CMOS logic at transition frequency of 10 to 100MHz.**

I. Introduction

With the widely spread of mobile, hand-held and wireless electronics devices, the demands for the innovations of low-power VLSI arise. For most of the digital circuits today, CMOS logic scheme has been the technology of choice for implementing low-power systems. As the clock and logic speeds increase to meet the new performance requirements, the energy requirement of CMOS circuits are becoming a major concern in the design of above devices.

Power dissipation in conventional CMOS primarily occurs during device switching. When a CMOS which consists of the pull-up (pMOS) and pull down (nMOS) networks connected to a load capacitance C_L is set into a logical "1" logic level, an energy of $E_{applied} = C_L {V_{dd}}^2$ is applied to the load [1]. Energy stored is half of the energy supplied, therefore the total dissipation as heat during charging and discharging, when the logic level is "0", is the same as $E_{total} = C_L {V_{dd}}^2$.

Energy dissipation in the channel resistance R is given as $E_{diss} = \left(\frac{RC_L}{\Delta T}\right) C_L {V_{dd}}^2$. For adiabatic charging, when ΔT, which means the time for the driving voltage to change from 0 V to V_{dd} is long, in theory, the energy dissipation is nearly zero. Adiabatic logic circuits also utilize AC power supplies to recycle the energy used to charge node capacitances in the circuit. As it dissipates less energy than the fundamental limit of static CMOS, adiabatic circuits are promising candidates for low-power circuits in the frequency range in which signals are digitally processed. In recent years, studies on adiabatic computing have been utilized for low-power systems and several adiabatic logic families have been proposed [1]–[15]. However, several weaknesses such as complex circuits, multiple power-clock supplies, nonadiabatic transitions that may compromise the energy savings and the logic gates are not well suited for CMOS implementation are seen.

In this paper, we propose a Two-Phase Adiabatic Static CMOS Logic (2PASCL) circuit. It can be directly converted from static CMOS circuits without drastically increasing the circuit complexity and transistor overheads. This circuit is emphasized on the recycle of the charges as two diodes are placed for the discharging. The functional of ripple carry adder based on 2PASCL is evaluated and energy dissipation is compared with CMOS at transition frequency of 10 to 100 MHz.

II. Two Phase Adiabatic Static CMOS Logic

Figure 1 shows a circuit diagram and waveforms illustrating the operation of the 2PASCL inverter. It resembles the static CMOS logic inverter but operates in a nearly adiabatic fashion. The first difference of 2PASCL compared to static CMOS logic gate is the two diodes, one from the output node to the power clock supply and another one is placed next to the nMOS logic to another power clock. The pMOS and nMOS diodes are used to recycle the charge from the output node. The other difference is that split-level sinusoidal power clock supplies, ϕ and $\overline{\phi}$ are used to replace the V_{dd} and the V_{ss}. From the simulation, we found that split-level sinusoidal gives a lower energy dissipation compared to trapezoidal power clock supply even if we set the T_{rise} and T_{fall} of the trapezoidal waveforms to a maximum values. By using two split-level sinusoidal waveforms which each peak-to-peak is 0.9 V, we can reduced the voltage difference, thus reducing the charging and discharging activities. Sinusoidal waveforms can also be generated with higher energy efficiency than trapezoidal waveforms [15].

The operation of 2PASCL is as follows. Let us consider the inverter logic circuit demonstrated in Fig. 1. The circuit

operation phase is divided into *evaluation* and *hold*.

In *evaluation* phase, when the output node Y is LOW and pMOS tree is turned ON, as ϕ swings up and $\overline{\phi}$ swings down, C_L is charged through pMOS transistor resulting the HIGH state at the output. When Y is LOW and nMOS is ON, no transition occurs. The same result gained when the output node is HIGH and pMOS is ON. When Y node is HIGH and nMOS is ON, discharging via nMOS and D2 resulting the output voltage decreased to V_t value before entering *hold* mode where the logical state is "0" [12]. For the *evaluation* mode where ϕ swings up and $\overline{\phi}$ swings down, the detailed operations are summarized by Table I.

TABLE I
OPERATION SUMMARY AT EVALUATION MODE

Prelim. state Y	ON transistor	Next state of Y
LOW	M1	HIGH
LOW	M2	LOW (no transition)
HIGH	M1	HIGH (no transition)
HIGH	M2	LOW

At *hold* mode where ϕ swings down and $\overline{\phi}$ swings up, due to the diodes, the state of Y when preliminary state is LOW remains unchanged. When the preliminary state of the output node is HIGH, it will change to V_t, the threshold voltage of the diode. At this point, discharging via D1 occurs.

From the operation of 2PASCL, less dynamic switchings are seen as circuit nodes are not necessarily charging and discharging every clock cycle which reduces the node switching activities significantly. The lower the switching activity reduces energy dissipation.

III. SIMULATION RESULTS AND DISCUSSION

A. Condition of simulation

The paper starts by examining the functional and energy dissipation of a simple logic gate, an inverter of 2PASCL as shown in Fig. 1. We use SPICE simulation with a 0.18 μm -1.8 V standard CMOS process. The W/L of nMOS and pMOS logic gates used is 0.6 μm/0.18 μm. A capacitive load C_L, of 0.01 pF is placed at output node Y. Bulks of pMOS and nMOS are connected to ϕ and $\overline{\phi}$ accordingly. The power supply clock frequencies are set to be 4 times higher than the transition frequency after considering energy dissipation results. Using split-level sinusoidal power clock driving voltage of 0.9 V peak-to-peak each, the result at 100 MHz transition frequency of 2PASCL inverter is shown in Fig. 1. The input signals are CMOS-compatible rectangular pulses. The top graph shows the split-level sinusoidal supply clock driving voltage. The second graph demonstrates the input signal and the third graph shows the output waveform of a correctly functioning inverter which was simulated with the SPICE. Its energy dissipation is calculated by integrating the voltage and current product value as follows:

$$E = \int_0^{T_s} \left(\sum_{i=1}^{n} (V_{pi} \times I_{pi}) \right) dt, \qquad (1)$$

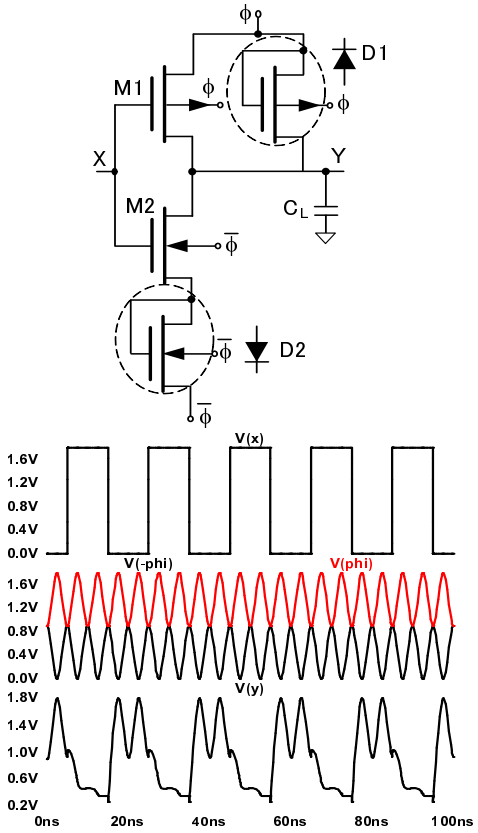

Fig. 1. 2PASCL inverter circuit and its waveforms.

where T_s is the period of the primary input signal, V_p is the power supply voltage, I_p is the power supply current and n is the number of power supply [12]. The energy in joule is then converted to watt by multiplying it with the input frequency.

TABLE II
CIRCUIT DATA FOR 2PASCL AND STATIC CMOS COMPARISON

Driving power voltage	0–1.8V
Split level ϕ and $\overline{\phi}$	0–0.9V, 0.9–1.8V
Frequency (input: driving voltage)	1:4
nMOS, pMOS (incl. diodes)	W/L : 0.6μm/0.18μm

Then, the simulation of 2PASCL based 1-bit full adder (FA) is carried out. As shown in Fig. 2, FA consists of exclusive-OR and NAND logic gates. Each exclusive-OR and NAND of 2PASCL is as demonstrated in Fig. 3 and Fig. 4 respectively. To verify the applicabilities of the proposed structure and 2PASCL property, a 4-bit ripple carry adder (RCA) has been designed and simulated. To enhance the performance evaluation, we simulate the frequency characteristics of power consumption for RCA of 2PASCL and the result is compared with CMOS. The transition frequencies simulated are from 10 to 100 MHz. The energy dissipation value is taken at the same time period for both circuits.

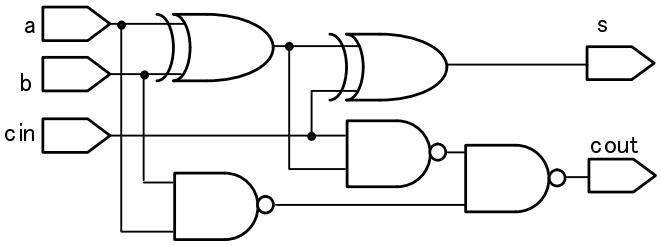

Fig. 2. Full adder.

B. Results and discussion

From the simulations, we have confirmed the functional of the 4-bit ripple carry adder 2PASCL logic circuits. The results are shown in Fig. 5. From the results, 2PASCL with split level sinusoidal clocking voltage gives a significant lower energy dissipation compared with conventional static CMOS for ripple carry adder. It also demonstrates a significant lower energy dissipation when transition frequency is simulated from 10 to 100 MHz which is shown in Fig. 6.

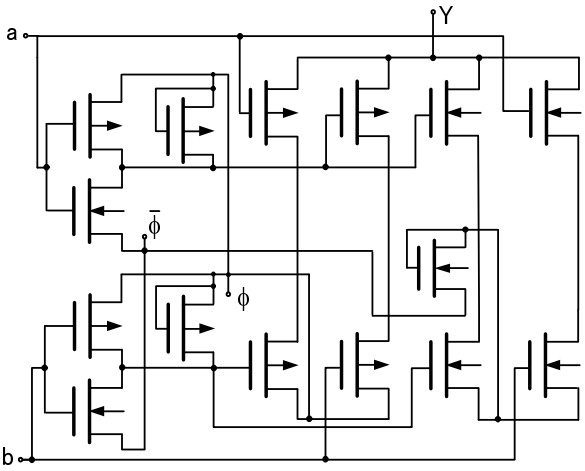

Fig. 3. Schematic for exclusive-OR logic of 2PASCL.

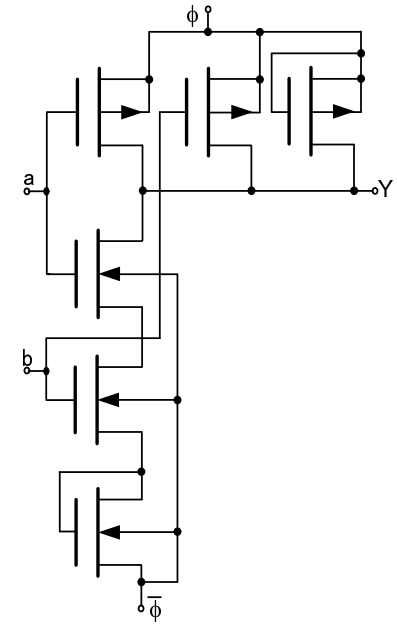

Fig. 4. Schematic for NAND logic of 2PASCL.

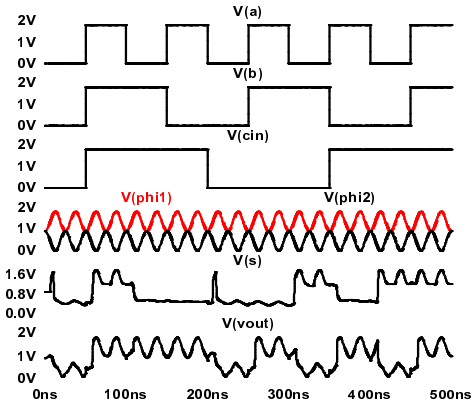

Fig. 5. Output waveforms for ripple carry adder of 2PASCL from the simulation result.

IV. Conclusion

This paper has described a simulation of Two-Phase clocked Adiabatic Static CMOS Logic (2PASCL). By implementing the adiabatic charging and energy recovery theory, 4-bit ripple carry adder (RCA) of 2PASCL is compared to RCA of static CMOS. Compared with static CMOS circuits, 2PASCL consumes much less power. For instance, at input frequency of 10 to 100 MHz, RCA of 2PASCL dissipates only 28.7% of the energy of static CMOS logic in average. From the results of other logic gates such as inverter chain [16], NAND, exclusive-OR and FA of 2PASCL which have been simulated, this logic scheme can be a viable candidate for ultra-low energy computing.

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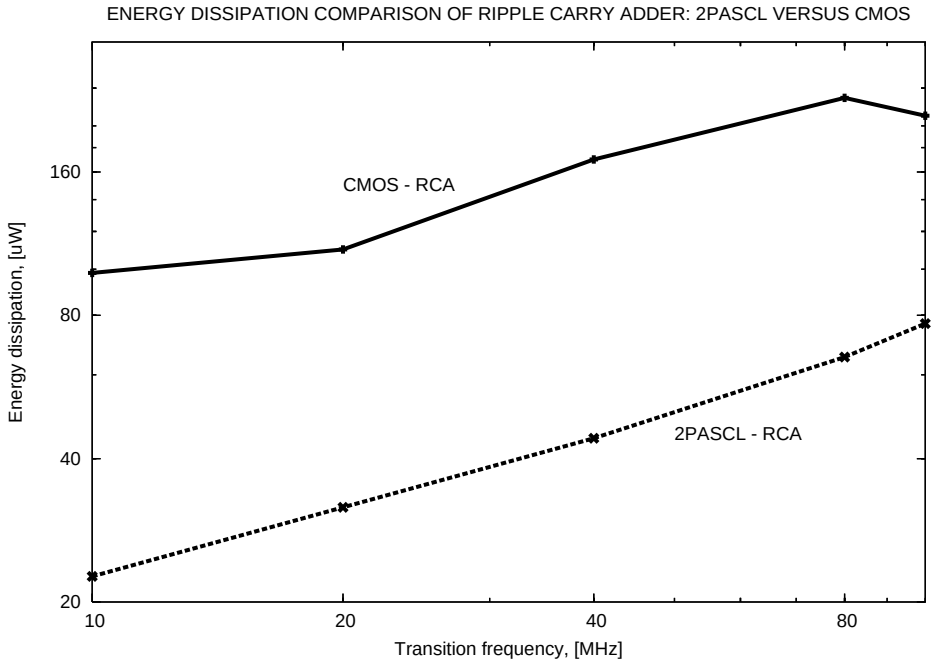

Fig. 6. Energy dissipation comparison with different transition frequency.

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