On Chip LC Resonator Circuit Using an Active Inductor for Adiabatic Logic

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***Abstract*—In this paper, we propose a LC resonator circuit using Hara's active inductor for adiabatic logic. The proposed circuit consists of four MOS-transistors Colpitts oscillator and an active inductor. This circuit require no inductor and can be produced two-phase sinusoidal clocking. From the simulation results, we show that the proposed circuit was operated as a 10 MHz, 3 V peak-to-peak LC resonant oscillator.**

I. Introduction

In the design of low-power VLSI circuits, adiabatic (or energy recovery) logic shows great potential, because they are able to break the lower limit of the energy dissipation in static CMOS which amounts to $CV_{dd}{}^2/2$. Numerous designs of adiabatic logic have been presented [1]–[10]. The driving of adiabatic logic requires adiabatic controlled sources of voltage. The adiabatic drivers fall into the following classes: resonant driver and staircase driver. The resonant driver generates the pulses from the natural oscillations of a resonator, with power recovery provided by a dc-voltage source. The generators of quasi-sinusoidal pulses can be built around the simplest resonator, namely, an LC circuit. Such a driver has been used in Refs. [2]–[7], and [9]. To generate quasi-sinusoidal pulses, lumped-parameter resonant drivers appear to be the best solution, since they offer the maximum efficiency. These drivers are totally adiabatic, provided that the resonator is free from dissipation. The main disadvantage of lumped-parameter resonant drivers is that they use off-chip chokes. The staircase driver was first proposed by L. J. Svensson and J. G. Koller [1], and then has been used in Refs. [8] and [10]. The staircase driver requires no inductors and can produce pulses of arbitrary shape. They can be fabricated as part of an IC. If the number of driving phases equals the number of voltage levels, no storage capacitors are needed, since the load capacitors can serve such a purpose. The main disadvantage of the staircase driver is that it includes many switches, which reduces its adiabatic rank.

In this paper, we present a LC resonant driver using an active inductor for adiabatic logic. The proposed resonant driver require no inductor and can produce two-phase sinusoidal clocking. The basis of the adiabatic logic is presented in Section II. In Section III, we present an on-chip LC resonant driver using an active inductor. We also show the performance of the proposed circuit. The conclusions are summarized in Section IV.

II. Adiabatic Logic

A. Conventional vs. Adiabatic Switching

The conventional switching can be understood by using a simple CMOS inverter. The CMOS inverter can be considered to consist of a pull-up and pull-down networks connected to a load (or internal) capacitance C. The pull-up and pull-down networks are actually MOS transistors in series with the same load C. Both transistors can be modeled by an ideal switch in series with a resistor which is equal to the corresponding channel resistance of the transistor in the saturation mode. When a conventional CMOS inverter is set into a logical "1" state, a charge $Q = CV_{DD}$ is delivered to the load and the energy which the supply applies is $E_{applied} = QV_{DD} = CV_{DD}{}^2$. The energy stored into the load C is a half of the supplied energy:

$$E_{stored} = \frac{1}{2}CV_{DD}{}^2. \tag{1}$$

The same amount of energy is dissipated during the discharge process in the NMOS pull-down network because no energy can enter the ground rail $Q \times V_{gnd} = Q \times 0 = 0$. From the energy conservation law, a conventional CMOS logic emits heat and, in this way, it wastes energy in every charge-discharge cycle:

$$\begin{aligned} E_{total} &= E_{charge} + E_{discharge} \\ &= \frac{1}{2}V_{DD}{}^2 + \frac{1}{2}CV_{DD}{}^2 \\ &= CV_{DD}{}^2. \end{aligned} \tag{2}$$

If the logic is driven by a certain frequency $f\ (= 1/T)$, where T is the period of the signal, then the power of the CMOS gate is determined as:

$$P_{total} = \frac{E_{total}}{T} = CV_{DD}{}^2 f. \tag{3}$$

The main idea in an adiabatic switching is that transitions are considered to be sufficiently slow so that heat is not emitted significantly. This is made possible by replacing the DC power supply by a resonance LC driver or oscillator. If a constant

current source delivers the $Q = CV_{DD}$ charge during the time period $\triangle T$, the energy dissipation in the channel resistance R is given by

$$\begin{aligned} E_{diss} &= P\triangle T \\ &= I^2 R\triangle T \\ &= \left(\frac{CV_{DD}}{\triangle T}\right)^2 R\triangle T. \end{aligned} \quad (4)$$

The above equation indicates that when the charging period $\triangle T$ is indefinitely long, in theory, the energy dissipation is reduced to zero. This is called an adiabatic switching [1].

B. 2PADCL

The 2PADCL inverter is shown in the top of Fig. 1(a), where the inverter is operated with complementary phases of power supply signals. The supply waveform consists of two modes, "evaluation" and "hold," as shown in the bottom of Fig. 1(a). Let us consider the adiabatic mode. When V_p and $\overline{V_p}$ are in evaluate mode, there is conducting path(s) in either PMOS devices or NMOS devices. Output node may evaluate from low to high or from high to low or remain unchanged, which resembles to the CMOS circuit. Thus, there is no need to restore the node voltage to 0 (or V_{DD}) every cycle. When V_p and $\overline{V_p}$ are in hold mode, Output node holds its value in spite of the fact that V_p and $\overline{V_p}$ are changing their values. We can find that such is the case by observing the function of diodes and the fact that the inputs of a gate have a different phase with the output. Circuits node are not necessarily charging and discharging every clock cycle, reducing the node switching activity substantially as shown in Fig. 1(b).

In the proposed 2PADCL circuits, energy dissipation is from the threshold voltage and transistor channel resistance. We use an RC model with a threshold voltage V_t to calculate the energy dissipation in transistor, which can be used estimate the energy consumption in adiabatic circuit. The energy dissipation of 2PADCL can be calculated as follows:

$$E = 2C_{gs}\left(V_p - 2V_d\right)V_d + C_{gs}\left(V_t - V_d\right)^2, \quad (5)$$

where C_{gs} is a gate-source capacitance in the next stage. Assume, $C_{gs} = 0.02$ pF, $V_t = V_d = 0.8$ V, and $V_p = 5$ V, then we have $E = 0.11$ pJ/cycle. Since 2PADCL gate is possible to maintain the output voltage without the load capacitor, its energy consumption can be reduced.

III. Power Clock Generator

A. Hara Active Inductor

Figures 2 and 3 show Hara's active inductor [11] and its small signal model, respectively. This circuit is indeed gyrator-C active inductor. The feedback operation of Hara's active inductor is as the followings: An increase of the input current will result in an increase in the voltage at the input node. Since the gate voltage is kept at V_{dd}, v_{gs} is reduced. This is turn lowers the current flowing out of the active inductor.

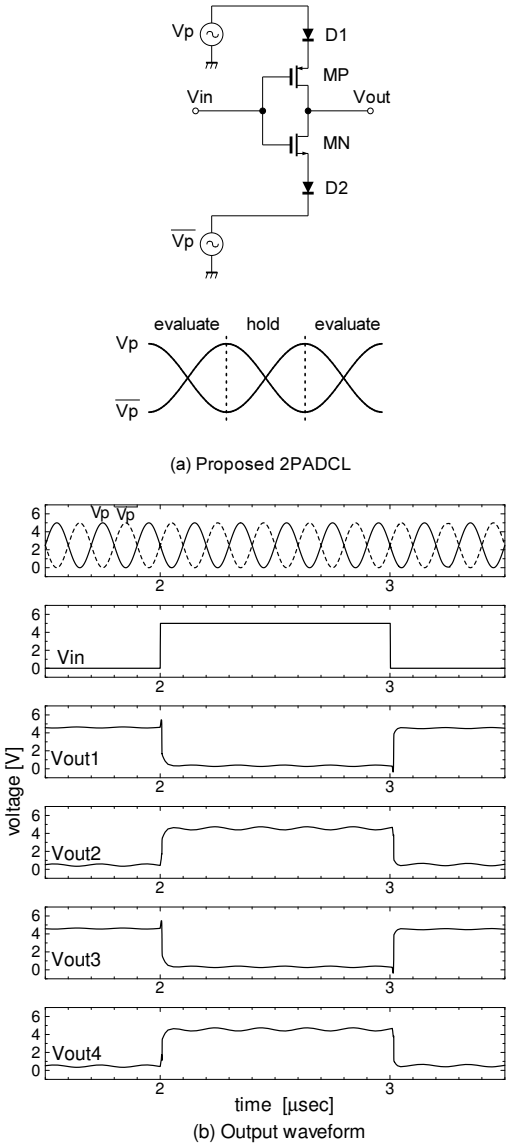


Fig. 1. 2PADCL inverter. (a) Structure and clock of the power supply. (b) Output waveform of the four-inverter chains.

The input impedance of the Hara's active inductor can be calcurated from its small signal equivalent model shown in Fig. 3

$$Z \approx \left(\frac{1}{RC_{gs}C_{gd}}\right)\frac{sRC_{gd}+1}{s^2 + s\dfrac{g_m}{C_{gs}} + \dfrac{g_m}{RC_{gs}C_{gd}}}, \quad (6)$$

where $gm \gg g_o$ and $C_{gs} \gg C_{gd}$ were utilized to simplify the results.

The self-resonant frequency ω_o and the frequency of the

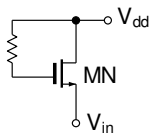


Fig. 2. Hara's active inductor.

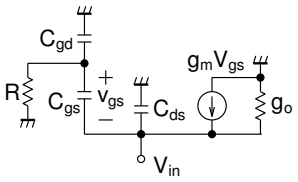


Fig. 3. Small signal model of Hara's Active Inductor.

zero ω_z of the active inductor are given by

$$\omega_o = \sqrt{\frac{g_m}{RC_{gs}C_{gd}}} = \sqrt{\omega_t \omega_z}, \quad (7)$$

$$\omega_z = \frac{1}{RC_{gd}}, \quad (8)$$

$$(9)$$

where

$$\omega_t = \frac{g_m}{C_{gs}}. \quad (10)$$

The network exhibits an inductor characteristic in the frequency range $\omega_z < \omega < \omega_o$. When C_{gd}, C_{sb}, and high-order effects are neglected, the inductance L and parastic series resistance R_s of Hara's active inductors are given by

$$R_s = \frac{g_m + R\left(\omega C_{gs}\right)^2}{g_m^2 + R\left(\omega C_{gs}\right)^2}, \quad (11)$$

and

$$L = \frac{\omega C_{gs}(g_m R - 1)}{g_m^2 + R\left(\omega C_{gs}\right)^2}. \quad (12)$$

Observe that

$$g_m R > 1 \quad (13)$$

is required to ensure $L > 0$. Under the condition $g_m R \gg 1$, Eqs. (11) and (12) can be written as

$$R \approx \frac{1}{g_m}, \quad (14)$$

and

$$L \approx \frac{C_{gs}R}{g_m}. \quad (15)$$

Figures 4 and 5 show a simple resonant equivalent circuit of Hara's active inductor and its dependence of the input impedance, respectively. The active inductor was implemented in an 1.2 μm CMOS n-well technology provided by On-Semi conductor and analyzed using PSPICE with BSIM3V3 device models.

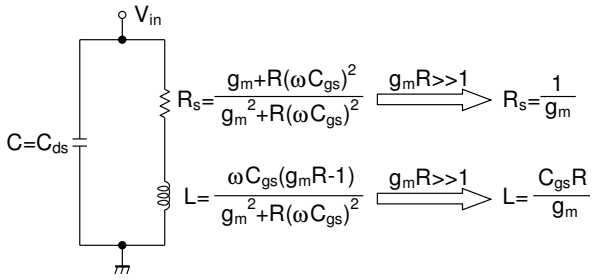
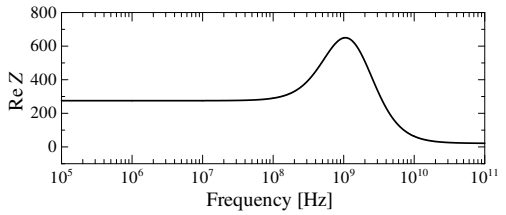
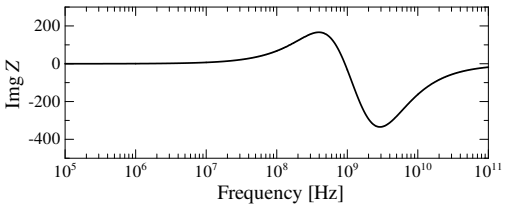


Fig. 4. Simple resonant equivalent circuit of Hara's active inductor.



(a) Real part impedance.



(b) Imaginary part impedance.

Fig. 5. Dependence of Z of Hara's active inductor.

B. Proposed On-chip Power Generator

The 2PADCL circuit has required two sinusoidal wave, V_p and $\overline{V_p}$. In this paper, we propose an LC resonant driver using Hara's active inductor. The proposed generator consists of four MOS-transistors Colpitts oscillator and an active inductor, as shown in Fig. 6.

If, at time t_0, $V_1 = 5$ V and $V_2 = 0$ V, then the inductor L will serve to pump charge from C_L and back again. The waveform presented across each capacitor will be a sinewave with an amplitude that decreases with time due to the resistive losses in the inductor and adiabatic circuits. To maintain the amplitude of the supply waveform, switches to the dc supply and ground are provided as shown (MP1 and MN2), and are activated at appropriate moments to top-up the system. The gates on these devices are driven by the resonant circuit itself. Note that in this circuit, there is only an inductor present in the high-current supply path between the two capacitors. The switches only carry the relatively low top-up current, minimizing the potential resistive losses in the circuit.

C. Simulation Results

The complete clock generator circuits was designed with the device parameters shown in Table I, and has a sinusoidal frequency of 10 MHz. The proposed circuit was tested by PSPICE simulation using a standard 1.2 μm CMOS process

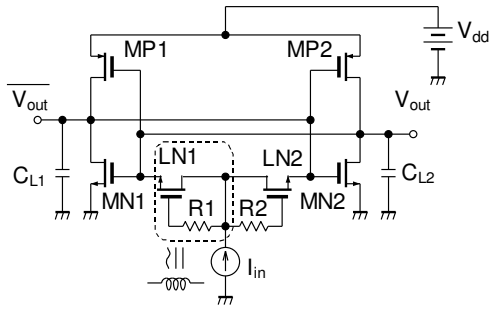


Fig. 6. Proposed on-chip LC resonance circuit.

TABLE I
DEVICE PARAMETER VALUES OF THE PROPOSED CIRCUIT.

MP1	$W/L = 1.2/1.2$	MP2	$W/L = 1.2/1.2$
MP1	$W/L = 1.2/1.2$	MP2	$W/L = 1.2/1.2$
LN1	$W/L = 13/4$	LN2	$W/L = 13/4$
$V_{dd} = 5$ V	$I_{in} = 400$ μA		
$R1 = 1$ MΩ	$R2 = 1$ MΩ	$C_{L1} = 0.1$ pF	$C_{L2} = 0.1$ pF

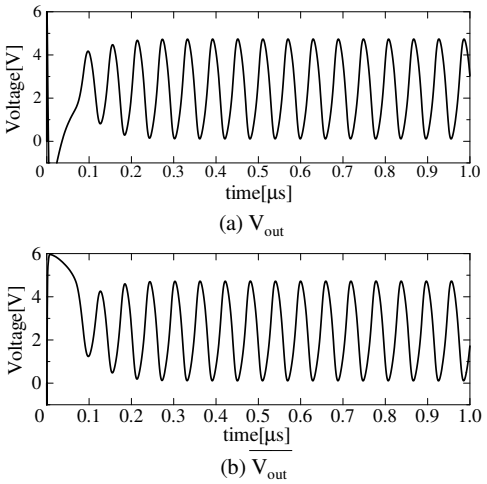


Fig. 7. Output waveform of the proposed LC circuit.

technology provided by VLSI Design and Education Center (VDEC), the University of Tokyo, with the collaboration by On-Semiconductor Corporation.

Figure 7 illustrates an output waveform of the proposed active LC circuit. From this figure, we found that the proposed circuit is operated as a 10 MHz, 3 V_{pp} LC resonant oscillator.

IV. CONCLUSION

In this paper, we have presented an on-chip resonant circuit using an active inductor for an adiabatic logic. The proposed circuit has used four MOS-transistors Colpitts oscillator and Hara's active inductor. Our simulation result has shown that the proposed circuit was operated as a 10 MHz, 3 V_{pp} LC resonant oscillator.

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