XOR Evaluation For 4×4-Bit Array Two-Phase Clocked Adiabatic Static CMOS Logic Multiplier

Nazrul Anuar
Graduate School of Engineering
Gifu University, 1-1 Yanagido,
Gifu-shi 501–1193 Japan
Email: n3814101@edu.gifu-u.ac.jp

Yasuhiro Takahashi and Toshikazu Sekine
Department of Electrical and Electronic Engineering
Gifu University, 1-1 Yanagido,
Gifu-shi 501–1193 Japan
Email:{yasut, sekine}@gifu-u.ac.jp

***Abstract*— This paper evaluates four designs of XOR employing our previously presented two-phase clocked adiabatic static CMOS logic (2PASCL) circuit techniques. 2PASCL XOR, which demonstrates the lowest power dissipation, is used for the 4×4-bit array 2PASCL multiplier. From our simulation results, at transition frequencies of 1 to 100 MHz, the 4×4-bit array 2PASCL multiplier shows a maximum of 55% reduction in power dissipation to that of a static CMOS.**

I. Introduction

In recent times, one of the major goals in VLSI design is a long battery operating life. In conventional CMOS circuits, power dissipation primarily occurs during device switching. Sudden flow of current through channel resistive elements resulting in one-half the supplied energy, i.e., $(\frac{1}{2})C_L V_{dd}^2$ dissipated at each transition. The innovation of low-power circuit systems by implementing the concept of adiabatic switching and energy recovery has been applied where several early adiabatic logic families have been proposed [1]–[4]. A few more papers on the applications of adiabatic logics [5]–[14] have been added subsequently. As it shows lower power dissipation than that in static CMOS circuits, adiabatic circuits are promising candidates for low-power circuits that can be operated in the frequency range in which signals are digitally processed.

At the earlier stage of the 2PASCL [15], we have designed, simulated, and compared the power consumption of 2PASCL NOT, 2NAND, 2XOR, and 2NOR to CMOS topology. 2PASCL fundamental logics significantly exhibit a lower power dissipation [16], [17]. In this paper, we design, simulate, and evaluate several new schematics of 2PASCL 2XOR. Then, a 4×4-bit array 2PASCL multiplier is simulated, and a comparison to CMOS multiplier is carried out. The simulations in this paper use SPICE implemented with 0.18 μm standard CMOS technology.

II. 2PASCL

A. Circuit Operation

Figure 1 shows a circuit diagram and waveforms illustrating the operation of the 2PASCL inverter [15]. A two-diode circuit is used; one diode is placed between the output node and power clock, and the other diode is placed adjacent to the nMOS logic circuit and connected to another power source.

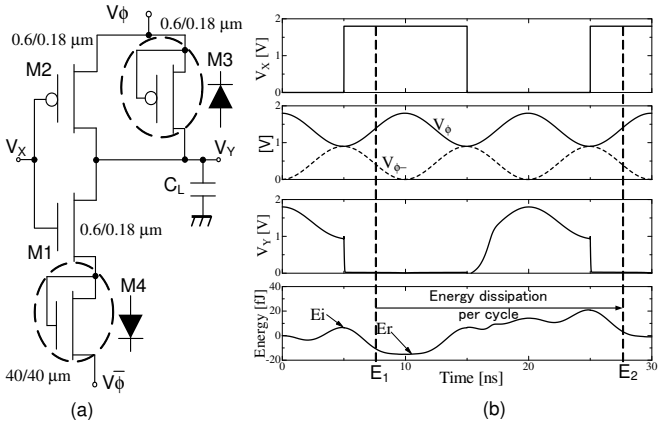

Fig. 1. (a) 2PASCL inverter circuit. (b) Waveforms from the simulation, transition frequency X=50 MHz, V_ϕ = $V_{\overline{\phi}}$ = 100 MHz.

Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes.

A novel method for reducing energy dissipation in a quasi-adiabatic 2PASCL involves the design of a charging path without diodes. In this case, during charging, current flows only through the transistor. Thus, the 2PASCL circuit is different from other diode-based adiabatic circuits, in which current flows through the diode and the transistor. With the aforementioned 2PASCL circuit, we can achieve high amplitude and reduce energy dissipation. In energy-recovery circuits, based on the energy conservation law– energy dissipated is equal to the total energy injected to the circuit, E_i and the energy received back from the circuit capacitance, E_r. This is shown in the energy graph in Fig. 1. Therefore in the simulation, the power dissipated is calculated by integrating the product of voltage and current divided by the period of the primary input signal, T as follows:

$$P = \frac{1}{T}\int_0^T \left(\sum_{i=1}^{n}(V_{pi}I_{pi})\right) dt, \qquad (1)$$

where V_p, the power supply voltage; I_p, the power supply current; and n, is the number of power supplies [13].

978-1-4244-7772-2/10/$26.00 ©2010 IEEE

TABLE I
2PASCL NOT LOGIC CIRCUIT OPERATION

Mode	Y_{-1}	pMOS	nMOS	Y
Evaluation	LO	ON	OFF	HI
	HI	OFF	ON	LO
Hold	HI	OFF	ON	No Transition

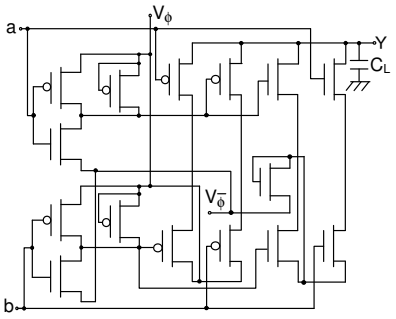

Fig. 2. 2PASCL 2XOR schematic (Dsg1).

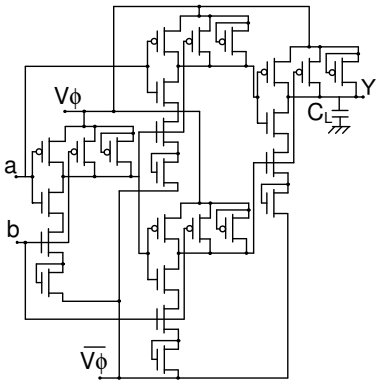

Fig. 3. 2PASCL 2XOR schematic (Dsg2).

The proposed system uses a two-phase clocking split-level sinusoidal power supply, wherein V_ϕ and $V_{\bar{\phi}}$ replace V_{dd} and V_{ss}, respectively. One clock is in phase while the other is inverted. The voltage level of V_ϕ exceeds that of $V_{\bar{\phi}}$ by a factor of $V_{dd}/2$. By using these two split-level sinusoidal waveforms, which have peak-to-peak voltages of 0.9 V, the voltage difference between the current-carrying electrodes can be minimized; consequently, power consumption can be suppressed. The substrates of the pMOS and nMOS transistors are connected to 1.8 V V_{dd} and V_{ss} respectively.

The circuit operation is divided into two phases, *evaluation* and *hold*. In the *evaluation* phase, V_ϕ swings up and $V_{\bar{\phi}}$ swings down. On the other hand, in the *hold* phase, $V_{\bar{\phi}}$ swings up and V_ϕ swings down. Let us consider the inverter logic circuit demonstrated in Fig. 1. The operation of the 2PASCL inverter is explained as follows:

1) *Evaluation* phase:
   a) When Y is LOW and the pMOS tree is turned ON, C_L is charged through the pMOS transistor; hence, Y is in the HIGH state.

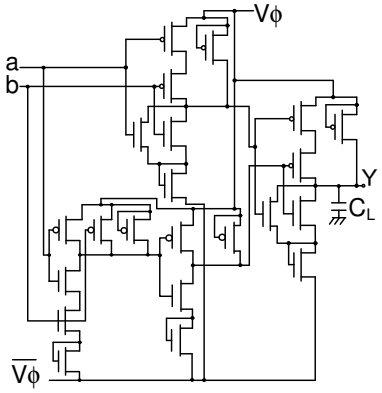

Fig. 4. 2PASCL 2XOR schematic (Dsg3).

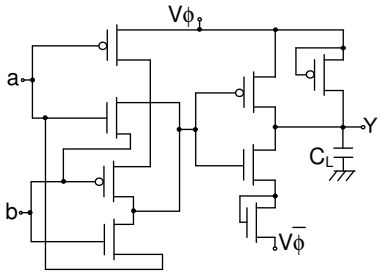

Fig. 5. 2PASCL 2XOR schematic (Dsg4).

   b) When node Y is HI and nMOS is ON, discharging via M1 and M4 occurs; hence , Y is in the LOW state.
2) *Hold* phase:
   a) At the point when the preliminary state of Y is HIGH and the pMOS is ON, no transition occurs.

Table I shows simplified 2PASCL NOT logic circuit operation. The number of dynamic switching transition occuring during the operation of the 2PASCL circuit decreases since the charging/discharging of the circuit nodes does not necessarily occur during every clock cycle. Hence, node switching activities are suppressed to a significant extent and consequently, energy dissipation is also reduced. One of the advantages of the 2PASCL circuit is that it can be made to behave like a static logic circuit.

B. Evaluation of 2PASCL 2XOR logic designs

Table II describes the details of all four 2PASCL 2XORs. Figure 2 shows the schematic of the first 2PASCL 2XOR logic circuit design. a and b are the inputs; V_ϕ and $V_{\bar{\phi}}$ are the power supply clocks; and Y is the output. In Fig. 3, 2XOR is presented using four 2NANDs logic. The combination of two 2NORs and one 2AND for 2XOR is shown in Fig. 4. Fig. 5 demonstrates the least gates of 2PASCL 2XOR. This schematic is derived from 2XOR CMOS presented in [18] to the 2PASCL 2XOR by adding the nMOS and pMOS diodes only at the NOT logic of the original 2XOR. Then, the split level sinusoidal power clocks are supplied to the circuit.

TABLE II
DETAILS OF 2XOR LOGIC

	Dsg1	Dsg2	Dsg3	Dsg4
No. of gates	15	24	22	8
Power diss., [μW] (f_T=1 MHz)	0.018	0.033	0.028	0.011

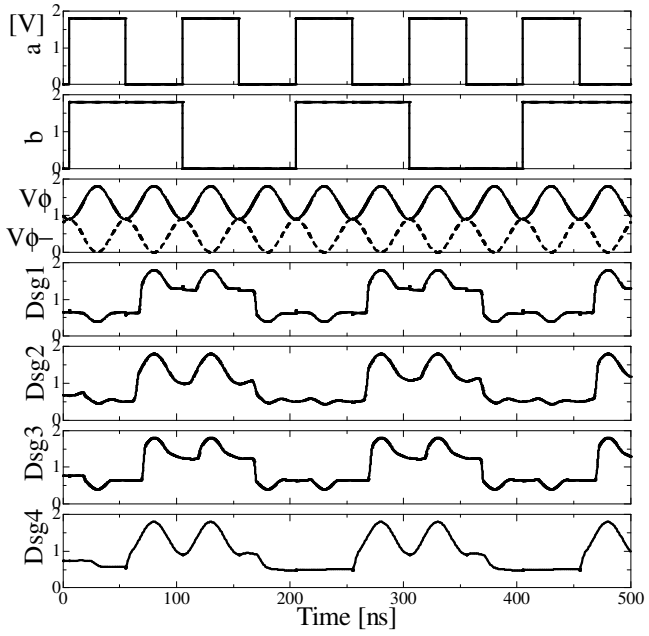

Fig. 6. The input, voltage clocks, and the output waveforms of all four 2PASCL 2XOR designs from the simulation.

In Fig. 6, we describe the output waveforms from the simulation results of each schematic designs. By comparing these four results at 10 MHz transition frequency, output waveforms generated by the schematic shown in Fig. 5 has the least glitches in the signal. In Table II, Dsg4 also shows relatively lower energy dissipation at transition frequency of 10 MHz. Thus, Dsg4 is used for the 4×4-bit array 2PASCL multiplier. Table III lists the main parameters used in the simulation.

C. 4×4-bit array 2PASCL multiplier

Figure 7 shows the diagram of 4×4-bit array multiplier which consists of sixteen ANDs, six full adders and four half adders logics. Load capacitance ranging from 0.01 to 0.1 pF are set at all outputs (p_0 to p_7). For fabrication, 2PASCL D-flipflops [15] are also used to capture all the 8-bit signals at the moment the clock is in HI state. In Fig. 8, we demonstrate the input and output waveforms of 50 MHz transition frequency 4×4-bit array 2PASCL multiplier. Figure 9 shows the power dissipation of 2PASCL multipliers which are about 55% less than CMOS multipliers. However, from our simulation results, 4×4-bit array 2PASCL multiplier only shows a good logic

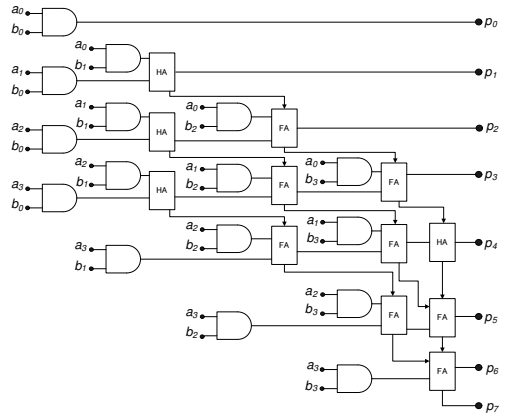

Fig. 7. Block diagram of 4×4-bit array multiplier.

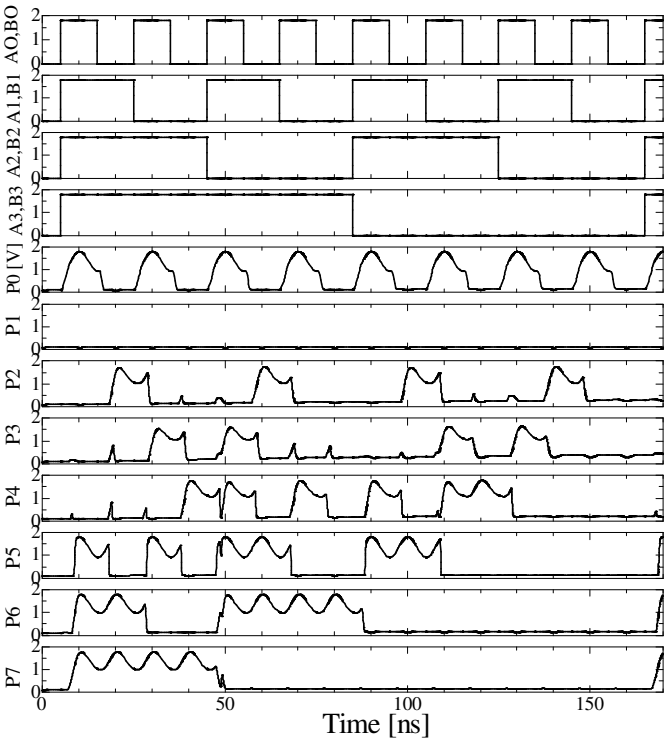

Fig. 8. Output waveforms of 4×4-bit array 2PASCL multiplier at 50 MHz transition frequency from the simulation.

functionality of up to 200 MHz transition frequency. We observed some signal degradations for transition frequency of more than 200 MHz. This is due to the charging time T which is much slower than conventional CMOS. T is also proportional to RC_L i.e. the longer the path, the larger T is needed. In Figure 10 we include the layout design of 2PASCL half adder and full adder using 1.2 μm CMOS process. Based on the simulation in 1.2 μm CMOS technology, at the transition frequency of 5 to 50 MHz, we saved up to 65% power dissipation compared with CMOS.

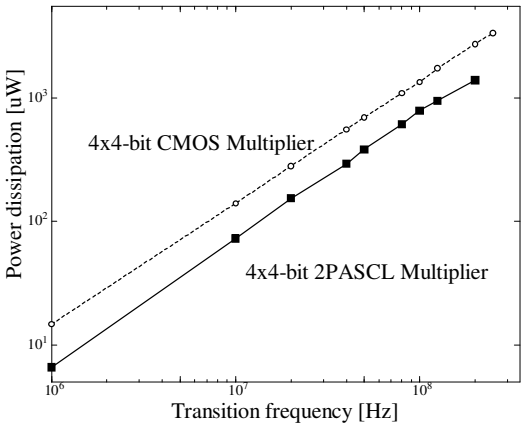

Fig. 9. Power dissipation comparison of 4×4-bit array 2PASCL multiplier and 4×4-bit array CMOS multiplier.

TABLE III
PARAMETER FOR ALL THE DESIGNS

W/L	0.6 μ/0.18 μ
W/L (nMOS diode)	40μ/40μ
V_ϕ, $V_{\overline{\phi}}$	0.9 V, 0.9 V
C_L	0.01 pF

D. Power supply clock

2PASCL has been powered by split-level sinusoidal power supply clocks [15]–[17]. To generate this, we have presented the proposed circuit in [19]. The generation of 1 MHz for the V_ϕ and $V_{\overline{\phi}}$ dissipates 16 μW from the power clock circuit. We evaluate other power clock circuits for higher efficiency which will be discussed in future publication.

III. CONCLUSION

In this paper we have designed and simulated a 4×4-bit array two-phase clocked adiabatic CMOS logic (2PASCL) multiplier circuit using the selected 2PASCL 2XOR from the evaluation. The simulation results show that power consumption in the 2PASCL multiplier is considerably less than that of a CMOS. For instance, when the input frequency is simulated from 1 to 100 MHz, the 2PASCL multiplier logic dissipates minimally as only half of the power dissipated by a static CMOS logic circuit. We believe that the proposed adiabatic logic circuit is advantageous for ultra low-energy computing applications.

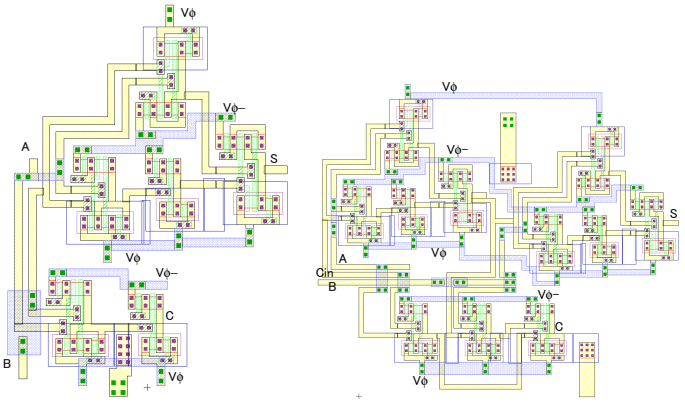

Fig. 10. Layout design of 2PASCL 1-bit half adder (left) and 2PASCL 1-bit full adder (right) using 1.2 μm CMOS technology.

REFERENCES

[1] W.C. Athas, L.J. Svensson, J.G. Koller, N. Tzartzains, and E. Y-C. Chou, "Low-power digital systems based on adiabatic-switching principles," *IEEE Trans. Very Large Scale Integration. (VLSI) Syst.*, vol. 2, no. 4, pp. 398–407, Dec. 1994.

[2] A. Kramer, J.S. Denker, S.C. Avery, A.G. Dickinson, and T.R. Wik, "Adiabatic Computing with the 2N-2N2D logic family," *Proc. IEEE Symposium on VLSI Circuits Dig. Tech. Papers*, pp. 25–26, June 1994.

[3] A.G. Dickinson and J.S. Denker, "Adiabatic dynamic logic," *IEEE J. Solid-States Circuits*, vol. 30, no. 3, pp. 311–315, Mar. 1995.

[4] Y. Moon and D.K. Jeong, "An efficient charge recovery logic circuit," *IEEE J. Solid-States Circuits*, vol. 31, no. 4, pp. 514–522, Apr. 1996.

[5] K.T. Lau and F. Liu, "Improved adiabatic pseudo- domino logic," *Electron. Lett.*, vol. 33, no. 25, pp. 2113–2114, 1997.

[6] V.I. Starosel'skii, "Reversible logic," *Mikroelektronika*, vol. 28, no. 3, pp. 213–222, 1999.

[7] K.A. Valiev and V.I. Starosel'skii, "A model and properties of a thermodynamically reversible logic gate," *Mikroelektronika*, vol. 29, no. 2, pp.83–98, 2000.

[8] K. Takahashi, and M. Mizunuma, "Adiabatic dynamic CMOS logic circuit," *Electronics and Communications in Japan Part II*, vol. 83, no. 5, pp. 50–58, April 2000 [*IEICE Trans. Electron.*, vol. J81-CII, no. 10, pp. 810–817, Oct. 1998].

[9] J. Marjonen, and M. Aberg, "A single clocked adiabatic static logic: a proposal for digital low power applications," *J. VLSI Signal Processing*, vol. 27, no. 27, pp. 253–268, Feb. 2001.

[10] Y. Ye, and K. Roy, "QSERL: Quasi-static energy recovery logic," *IEEE J. Solid-States Circuits.*, vol. 36, no. 2, pp. 239–248, Feb. 2001.

[11] V.I. Starosel'skii, "Adiabatic logic circuits: A review," *Russian Microelectronics*, vol. 31, no. 1, pp. 37–58, 2002.

[12] S. Kim, C.H. Ziesler, and M.C. Papaefthymiou, "Charge-recovery computing on silicon," *IEEE Trans. on Computers*, vol. 54, no. 6, pp. 651–659, Jun. 2005.

[13] Y. Takahashi, Y. Fukuta, T. Sekine, and M. Yokoyama, "2PADCL: Two phase drive adiabatic dynamic CMOS logic," in *Proc. IEEE APCCAS*, pp. 1486–1489, Dec. 2006.

[14] C. Siyong, et al, "Analysis and design of an efficient irreversible energy recovery logic in 0.18μm CMOS," *IEEE Trans. Circuits and Syst.*, vol.55, no. 9, pp. 2595–2607, Oct. 2008.

[15] N. Anuar, Y. Takahashi and T. Sekine, "Two phase clocked adiabatic static CMOS logic," *in Proc. IEEE SOC 2009*, pp.83–86, Oct. 2009.

[16] N. Anuar, Y. Takahashi and T. Sekine, "4-bit ripple carry adder of two-phase clocked adiabatic static CMOS logic," *in Proc. IEEE TENCON 2009*, THU4.P.16, Nov. 2009.

[17] N. Anuar, Y. Takahashi and T. Sekine, "Fundamental logics based on two phase clocked adiabatic static logic," *in Proc. IEEE ICECS 2009*, pp.503–506, Dec. 2009.

[18] J.M. Wang, S.C. Fang and W.S. feng. "New efficient designs for XOR and XNOR functions on the transistor level," *IEEJ. Solid-States Circuits*, vol. 29, no. 7, pp. 780–786, July. 1994.

[19] N. Anuar, Y. Takahashi and T. Sekine, "Two phase clocked adiabatic static CMOS logic and its logic," *J. Semiconductor Technology and Science*, vol. 10, no. 1, pp. 1–10, Mar. 2010.