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LOW-POWER 4×4-BIT ARRAY TWO-PHASE CLOCKED ADIABATIC STATIC CMOS LOGIC MULTIPLIER

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Abstract

The present study evaluates four designs of XOR using our previously reported two-phase clocked adiabatic static CMOS logic (2PASCL) circuit techniques. 2PASCL XOR, which demonstrates the lowest power dissipation, is used for a 4×4-bit array 2PASCL multiplier. Based on simulation results obtained using 0.18-μm standard CMOS technology, at transition frequencies of 1 to 100 MHz, the 4×4-bit array 2PASCL multiplier exhibits a maximum power dissipation that is 55% lower than that of a static CMOS. These results indicate that 2PASCL technology can be advantageous when applied to low-power digital devices operated at low frequencies, such as radio-frequency identification (RFID) tags, smart cards, and sensors.

Keywords and phrases : low-power, adiabatic logic circuit, power supply clock, power dissipation, adiabatic XOR logic design.

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1. Introduction

In recent years, various energy-recovery circuits with adiabatic circuitry for ultra-low power implementation have been presented [1]-[21]. Adiabatic charging [6] is a principle whereby charge transfer occurs without generating heat. The energy advantage can be understood by assuming a constant current source that delivers the charge $C_L V_{dd}^2$ over time *T*. The dissipation through the channel resistance *R* is then $E_{diss} = \left(\frac{RC_L}{T}\right) C_L V_{dd}^2$ [13]. Theoretically, it is possible to reduce the dissipation to an arbitrary degree by increasing the switching time to ever-larger values. Conventional adiabatic logic circuits [6]-[8], [10], [12]-[14], [17], [18], [21] exhibit much less power dissipation than the static CMOS circuit. For instance, at a clock input of 10 MHz, efficient charge recovery logic (ECRL) [12] dissipates only 16% of the energy of the static CMOS logic in a chain inverter application. However, most of these circuits require multiphase power clocks, and a number of problems, such as complicated clock design and increased energy dissipation due to the power clocks, are encountered. Furthermore, for single-phase and two-phase clock circuits, diode-based families [7], [10], [14], [17], [18], [21] have several disadvantages, including output amplitude degradation and energy dissipation across the diodes in the charging path [5].

At an earlier stage of the 2PASCL [1], we designed, simulated, and compared the power consumption of 2PASCL NOT, 2NAND, 2XOR, and 2NOR to CMOS topology. Furthermore, we discussed the pros and cons of 2PASCL compared to other proposed adiabatic logics that are easily derived from CMOS in [5]. 2PASCL fundamental logics exhibit significantly lower power dissipation [2]-[3].

In the present paper, we design, simulate, and evaluate several new 2PASCL 2XOR schematics. A 4×4-bit array 2PASCL multiplier is then simulated using 0.18-μm standard CMOS technology using a new 2PASCL 2XOR. The 2PASCL multiplier and CMOS multiplier are then compared. 2PASCL technology can be advantageous when applied to low-power digital devices operated at low frequencies, such as radio-frequency identification (RFID) tags, smart cards, and sensors.

The remainder of the present paper is organized as follows. Section 2 describes the circuit operation of 2PASCL. The simulation results of 2XOR and the 4×4-bit array 2PASCL multiplier are presented in Section 3. Finally, Section 4 presents concluding remarks and a discussion of future research.

2. 2PASCL

2.1. Circuit operation

Figure 1 shows a circuit diagram and waveforms illustrating the operation of the 2PASCL inverter [1]. The waveforms in Figure 1(b) are the input, split-level sinusoidal power supply clocks, and the output. The power supply clocks used in 2PASCL are V_{ϕ} and $V_{\bar{\phi}}$, where

$$V_{\phi} = \frac{V_{dd}}{4}\sin(\omega_0 t + \theta) + \frac{3}{4}V_{dd}, \tag{1}$$

$$V_{\bar{\phi}} = -\frac{V_{dd}}{4}\sin(\omega_0 t + \theta) + \frac{1}{4}V_{dd}. \tag{2}$$

The instantaneous energy dissipation is shown in the bottom graph of Figure 1(b). In energy-recovery circuits, based on the energy conservation law, the energy dissipated is equal to the total energy injected to the circuit, E_i, and the energy received back from the circuit capacitance, E_r. This is confirmed by the energy dissipation graph of Figure 1(b).

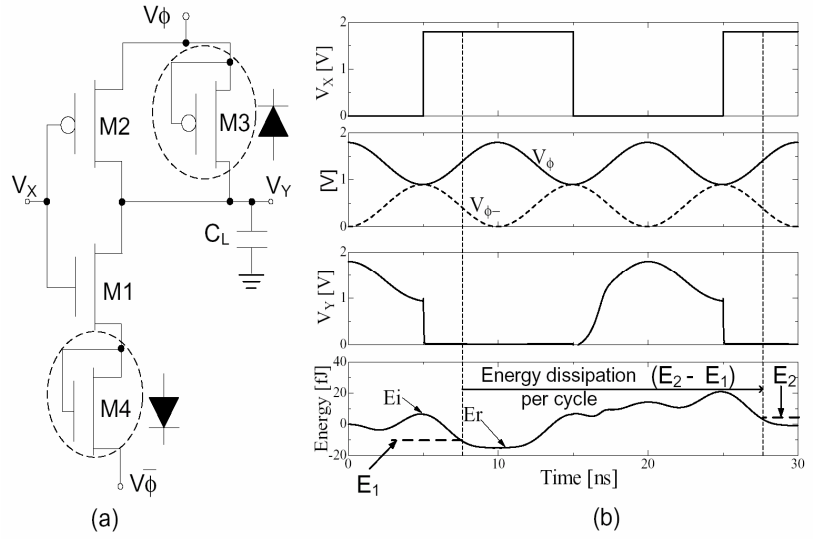

Figure 1. (a) 2PASCL inverter circuit. (b) Waveforms obtained in the simulation (transition frequency of V_X is 50 MHz and V_{ϕ}, $V_{\bar{\phi}}$ is 100 MHz).

The circuit operation is divided into two phases, namely, *evaluation* and *hold*. In the *evaluation* phase, V_{ϕ} swings up and $V_{\bar{\phi}}$ swings down, whereas in the *hold* phase, $V_{\bar{\phi}}$ swings up and V_{ϕ} swings down. Let us consider the inverter logic circuit demonstrated in Figure 1. The operation of the 2PASCL inverter is explained as follows:

(1) *Evaluation* phase:

(a) When *Y* is LOW and the pMOS tree is turned ON, C_L is charged through the pMOS transistor (M2). Hence, *Y* is in the HIGH state.

(b) When node *Y* is HI and nMOS is ON, discharging via M1 and M4 occurs. Hence, *Y* is in the LOW state.

(2) *Hold* phase:

(a) When the preliminary state of *Y* is HIGH and M2 is ON, no transition occurs.

Table 1 shows the simplified 2PASCL NOT logic circuit operation. The number of dynamic switching transitions occurring during the operation of the 2PASCL circuit decreases, because the charging/discharging of the circuit nodes does not necessarily occur during every clock cycle. Hence, node switching activities are suppressed to a significant extent, and, consequently, energy dissipation is also reduced. One of the advantages of the 2PASCL circuit is that this circuit can be made to behave as a static logic circuit.

Table 1. 2PASCL NOT logic circuit operation

Mode	Y_{-1}	pMOS	nMOS	*Y*
Evaluation	LO	ON	OFF	HI
	HI	OFF	ON	LO
Hold	HI	OFF	ON	No Transition

3. Simulation Results

3.1. Evaluation of 2PASCL 2XOR logic designs

Figure 2 shows the schematic of the first 2PASCL 2XOR logic circuit design

[5]. Here, *a* and *b* are the inputs, V_{ϕ} and $V_{\overline{\phi}}$ are the power supply clocks, and *Y* is the output. In Figure 3, 2XOR is presented using four 2NANDs logic. The combination of two 2NORs and one 2AND for 2XOR is shown in Figure 4. The schematic of Figure 5 shows the 2PASCL 2XOR having the fewest transistors. This 2PASCL 2XOR schematic is derived from 2XOR CMOS, which has been proposed by Wang et al. [20], by adding nMOS and pMOS diodes only at the NOT logic of the original 2XOR. The split level sinusoidal power clocks are then supplied to the circuit. Table 2 describes the four 2PASCL 2XORs in detail. As shown in Table 2, the number of transistors has been reduced from 15 to 8 in 2XOR. The MOSFETs in both 2PASCL and CMOS can be modeled as an ideal switch in series with a resistor *R* in order to represent the sum of the effective channel resistance of the switch and the interconnect resistance. We reduced the total resistance by minimizing the number of transistors and, consequently, reduced the power dissipation. Table 3 lists the main parameters used in the simulation.

Table 2. Details of 2XOR logic

	Dsg 1	Dsg 2	Dsg 3	Dsg 4
No. of gates	15	24	22	8
Power diss., $[\mu W](f_T = 1\,\text{MHz})$	0.018	0.033	0.028	0.011

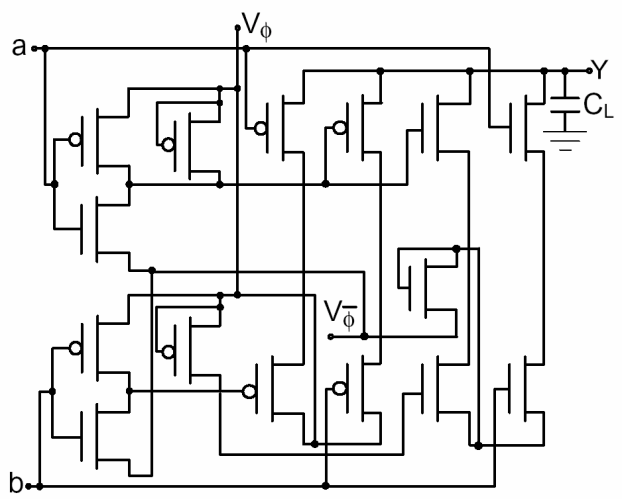

Figure 2. 2PASCL 2XOR schematic (Dsg 1).

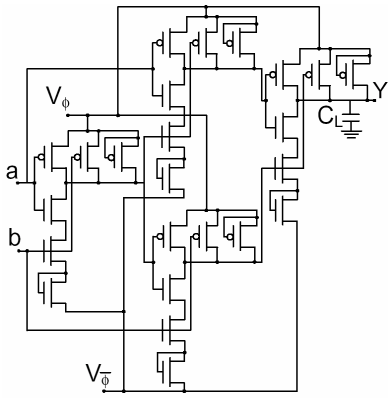

Figure 3. 2PASCL 2XOR schematic (Dsg 2).

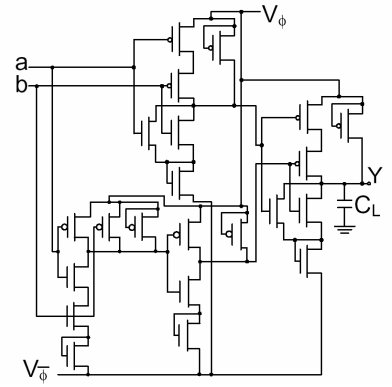

Figure 4. 2PASCL 2XOR schematic (Dsg 3).

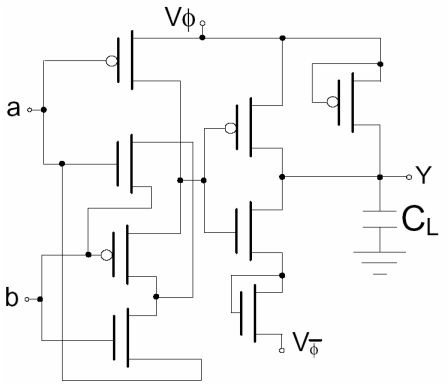

Figure 5. 2PASCL 2XOR schematic (Dsg 4).

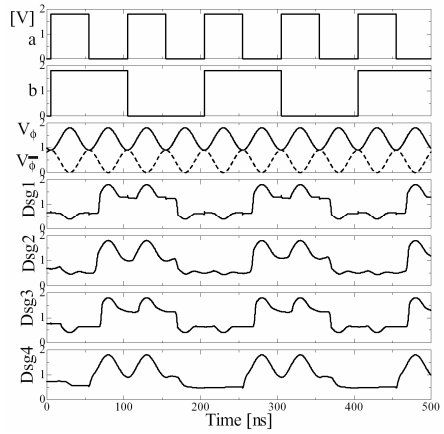

Figure 6. The input, power supply clocks, and output waveforms of the four 2PASCL 2XOR designs obtained from the simulation.

Table 3. Parameters for all designs

W/L	$0.6\,\mu/0.18\,\mu$
W/L (nMOS diode)	$40\mu/40\mu$
V_{ϕ}, $V_{\bar{\phi}}$	0.9 V, 0.9 V
C_L	0.01 pF

In Figure 6, we describe the output waveforms obtained from the simulation results for each schematic design. Comparing these four results at a transition frequency of 1 MHz reveals that the output waveforms generated by the schematic shown in Figure 5 has the fewest glitches in the signal. In Table 2, Dsg 4 also exhibits relatively lower energy dissipation at a transition frequency of 10 MHz. This is due to the shorter transmission path and, consequently, the reduced signal degradation. Thus, Dsg 4 is used for the 4×4-bit array 2PASCL multiplier. In the simulation, the power dissipated is calculated by integrating the product of voltage and current divided by the period of the primary input signal, *T*, as follows:

$$P = \frac{1}{T}\int_0^T \left(\sum_{i=1}^{n} (V_{pi} I_{pi}) \right) dt, \tag{3}$$

where V_p is the power supply voltage, I_p is the power supply current, and *n* is the number of power supplies [18].

3.2. 4×4-bit array 2PASCL multiplier

Figure 7 shows a diagram of the 4×4-bit array multiplier, which consists of 16 ANDs, 6 full adders, and 4 half adders. Load capacitance ranging from 0.01 to 0.1 pF are set at all outputs $(p_0$ to $p_7)$. For fabrication, 2PASCL D-flipflops [1] are also used to capture all of the 8-bit signals at the moment the clock is in the HI state. In Figure 8, we demonstrate the input and output waveforms of the 50 MHz transition frequency 4×4-bit array 2PASCL multiplier. Based on these results, we confirm that the 4×4-bit array 2PASCL multiplier is functioning correctly. However, a signal glitch occurs at outputs p_2 through p_4. Figure 9 shows the power dissipation of the 2PASCL multiplier, which is approximately 55% lower than that of a CMOS multiplier of the same transistor size, $W/L = 0.6/0.18\,\mu$m. However, based on our simulation results, the 4×4-bit array 2PASCL multiplier only exhibits good logic functionality at transition frequencies of up to 200 MHz, and signal degradation was observed for transition frequencies of greater than 200 MHz. This is due to the charging time, *T*, which is much slower than that of the conventional CMOS. Moreover, T is proportional to RC_L, i.e., the longer the path, the greater the required *T*. These input frequencies are adequate for the applications mentioned in Section 1. A multiblock layout is shown in Figure 10. One D-flipflop is connected to each of outputs p_0 through p_7. We fabricated a 4×4-bit array 2PASCL multiplier using 1.2-μm CMOS technology. The chip image is shown in Figure 11 and the chip specifications are listed in Table 4.

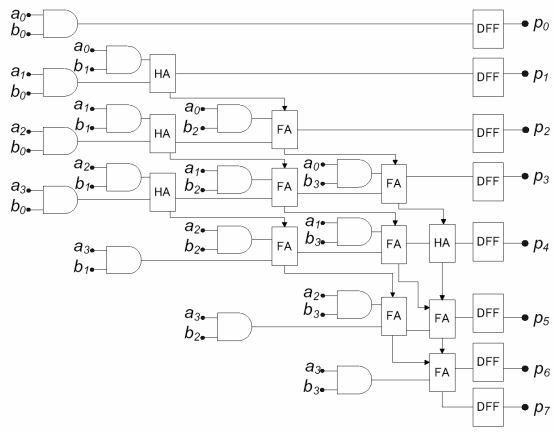

Figure 7. Block diagram of the 4×4-bit array 2PASCL multiplier with D-flipflops at the outputs.

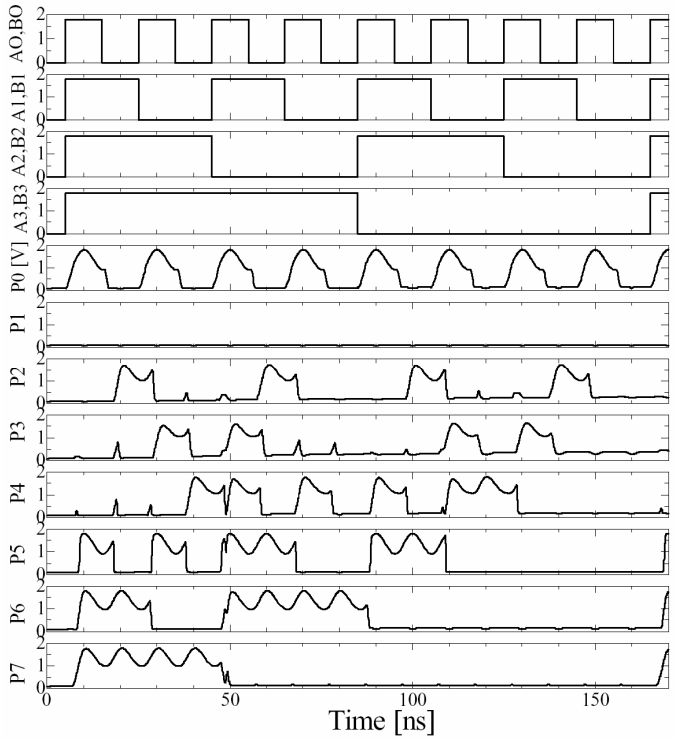

Figure 8. Output waveforms of the 4×4-bit array 2PASCL multiplier at a transition frequency of 50 MHz obtained from the simulation.

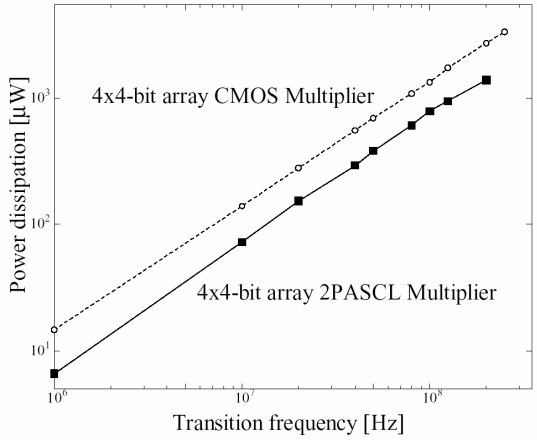

Figure 9. Power dissipation comparison of the 4×4-bit array 2PASCL multiplier and the 4×4-bit array CMOS multiplier.

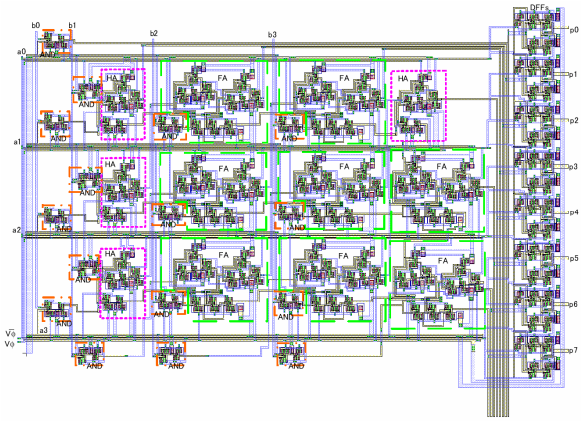

Figure 10. Layout of the 4×4-bit array 2PASCL multiplier.

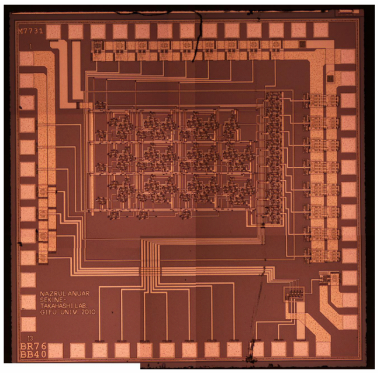

Figure 11. Chip image of the 4×4-bit array 2PASCL multiplier using a 1.2-μm CMOS process.

Table 4. Chip specifications

Technology	1.2-μm CMOS 2-metal, 2-poly
Power Voltage	5.0 V
Core Size	$1354\ (\mathrm{W}) \times 997\ (\mathrm{H})\mu\mathrm{m}^2$
No. of transistors	992
Dynamic Operating Frequency	5-50 MHz (from simulation)
Dynamic Power Dissipation	4 mW@10 MHz (from simulation)

3.3. Power supply clock

Previously, 2PASCL has been powered by split-level sinusoidal power supply clocks [1]-[3]. This design for the proposed circuit was presented in [5]. The generation of 1 MHz for V_{ϕ} and $V_{\bar{\phi}}$ dissipates 16 μW from the power clock circuit. We evaluated other power clock circuits for higher efficiency, as will be discussed in a future publication.

4. Conclusion

In the present study, we have designed and simulated a 4×4-bit array two-phase clocked adiabatic CMOS logic (2PASCL) multiplier circuit using a 2PASCL 2XOR selected based on the simulation results of the power dissipation, the output waveforms, and the optimal number of transistors. The simulation results show that power consumption of the 2PASCL multiplier is considerably lower than that of the CMOS multiplier. For instance, when the input frequency is simulated from 1 to 100 MHz, the 2PASCL multiplier logic dissipates minimally only half of the power dissipated by a static CMOS logic circuit. We believe that the proposed adiabatic logic circuit is advantageous for ultra-low-energy computing applications. In the future, we intend to further evaluate the cause of the signal glitches in 2PASCL.

Acknowledgements

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