40 MHz LC Voltage driver and clock circuit for 2PASCL

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Abstract

The paper presents two complementary split-level sinusoidal power supply clock circuit for Two-Phase Adiabatic Static CMOS Logic circuit (2PASCL). We investigate the most suitable scheme which provide the highest efficiency for energy recovery power supply clocks using SPICE simulation.

1 Introduction

We have designed and simulated the complementary split level sinusoidal waveforms to drive and used as clock for 2PASCL. It is using the LC circuit with $V_{dd}/2$ power voltage connected in series to create the ϕ which is $V_{dd}/2$ V higher than $\overline{\phi}$. However, the result of the energy dissipation shows that it is 85.9 % higher compared when using the default clock in SPICE simulation. The clock needs to be redesigned with appropriate parameters in order to reduce the energy consumption in the 2PASCL logic circuits.

In this paper, we design another LC to generate 40 MHz split level sinusoidal waveforms. The clocks are used to drive the proposed 2PASCL logic circuit with 10 MHz transition frequency. Then, the power dissipation compared to the default sine wave from the SPICE simulator.

2 Simulation and results

As shown in Fig. 1, a circuit consist of DC power voltage, inductor L, capacitor C and nMOS transistor of W/L of $72.4\mu/9.8\mu$ is used to generate a complementary split level sinusoidal driving voltage and clock for 2PASCL circuit. One is in phase and one is inverted. To generate a $V_{dd}/2$ higher of $\overline{\phi}$, as demonstrated in Fig. 4, $V_{dd}/2$ is added in series to the output.

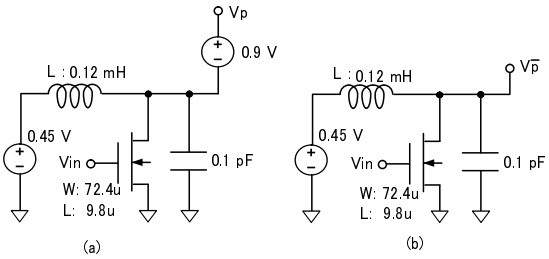

Fig. 1 (a) Circuit to generate ϕ (b) Circuit to generate $\overline{\phi}$.

The result of the simulation is as plotted in Fig. 5

The result of the simulation using default voltage is as plotted in Fig. 6

3 Conclusion

We have designed and simulated the complementary split level sinusoidal waveforms to drive and used as clock for 2PASCL. It is using the LC circuit with $V_{dd}/2$ power voltage connected in series to create the ϕ which is $V_{dd}/2$ V higher than $\overline{\phi}$. However, the result shows that the reqired 40 MHz is not able to achieved with

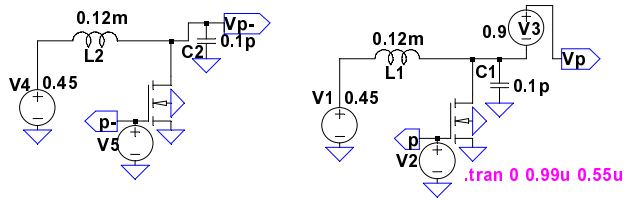

Fig. 2 SPICE schematic of the LC circuit with values.

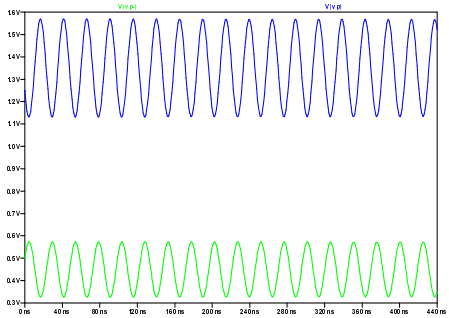

Fig. 3 Independent output result of 40 MHz clock. Bigger amplitude cannot be achieved, thus the adiabatic switching clocks are not feasible.

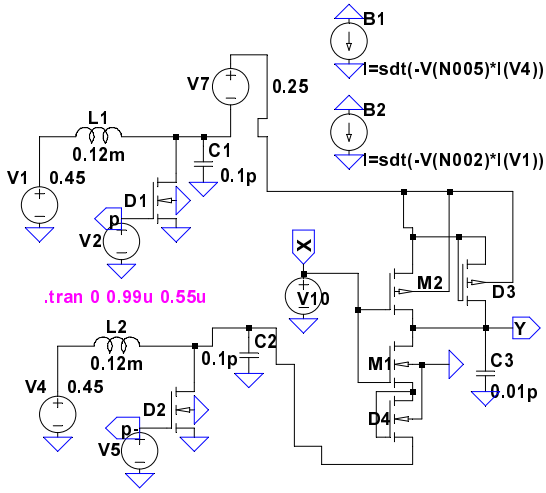

Fig. 4 SPICE diagram of the clock voltage driver with values of each component is detailed.

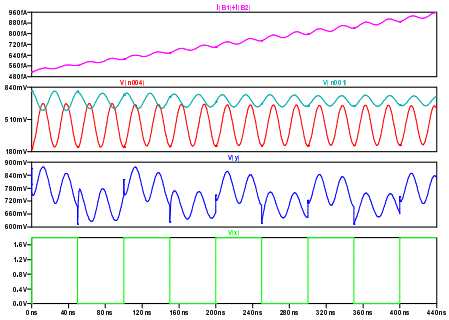

Fig. 5 Simulation output waveforms, the result of the proposed voltage power clock circuit. f=40 MHz. The V_p on the second graph has been reduced to meet the requirement of adiabatic switching

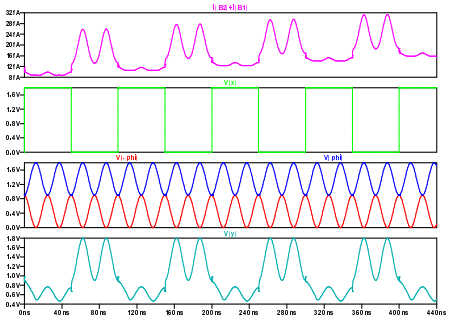

Fig. 6 Simulation output waveforms, the result of the default voltage power clock circuit. f=40 MHz

the existing parameter setting. Further evaluation on the parameters not to be done in future.