SR and Clocked D Flip-flops Using 2PASCL : Functionality and Energy Dissipation Comparison with Static CMOS

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Abstract

The paper presents SPICE simulations on SR (set-reset) flip-flop and clocked D (Data) flip-flop based on 2PASCL circuit. The functionality and the energy dissipation comparison between 2PASCL based and CMOS based Flip Flop is carried out. From the results, 2PASCL based FLIP FLOP can save up to 72% of energy dissipated from CMOS Flip Flop.

1 Introduction

We have designed and simulated 4-bit Ripple Carry Adder (RCA) using 2PASCL. From the simulation results, 2PASCL based RCA has 71% lower energy dissipation. However, only one application is not enough to determine the performance of 2PASCL. In this paper, we design SR and Clocked D Flip Flop using 2PASCL technique and the energy dissipation is compared to CMOS.

2 SR and Clocked D flip-flops

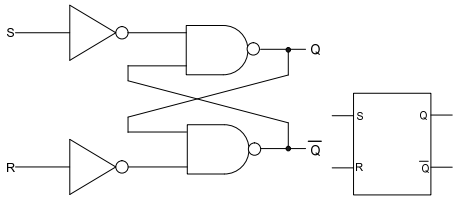

Fig. 1 Set-reset flip-flop.

The fundamental latch is the simple SR flip-flop, where S and R stand for set and reset respectively. It can be constructed from a pair of cross-coupled NAND or NOR logic gates. The stored bit is present on the output marked Q.

Table 1 SR Flip-Flop operation (characteristic table)

S	R	Action
0	0	Keep state
0	1	Q=0
1	0	Q=1
1	1	Unstable condition

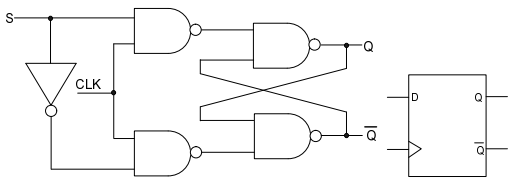

Fig. 2 Clocked D flip-flop.

The Q output always takes on the state of the D input at the moment of a rising clock edge (or falling edge if the clock input is active low). D flip-flop, where D means data, since the output takes the value of the D input or Data input and Delays it by one clock count. D flip-flop can be interpreted as a primitive memory cell, zero-order hold, or delay line [1]

Table 2 D Flip-Flop operation (characteristic table)

Clock	D	Q	Q_{prev}
Rising edge	0	0	X
Rising edge	1	1	X
Non-Rising	X	Q_{prev}	

3 Simulation and results

3.1 SR flip-flop

3.1.1 CMOS based

CMOS based set-reset flip flop is as in Fig. 3. The output waveforms and the energy calculation in joule is shown on the bottom of the same figure.

3.1.2 2PASCL based

2PASCL based set-reset flip flop is as in Fig. 4. The output waveforms and the energy calculation in joule is shown on the bottom of the same figure.

3.2 Clocked D flip-flop

3.2.1 CMOS based

CMOS based clocked D flip flop is as in Fig. 5. The output waveforms and the energy calculation in joule is shown on the bottom of the same figure.

3.2.2 2PASCL based

2PASCL based clocked D flip flop is as in Fig. 5. The output waveforms and the energy calculation in joule is shown on the bottom of the same figure.

3.3 Energy dissipation comparison

From the simulation results, the energy dissipation of both flip-flops using both CMOS and 2PASCL circuit techniques are as follows:

4 Conclusion

We have designed and simulated the SR and clocked D flip-flops using 2PASCL circuit technique. From

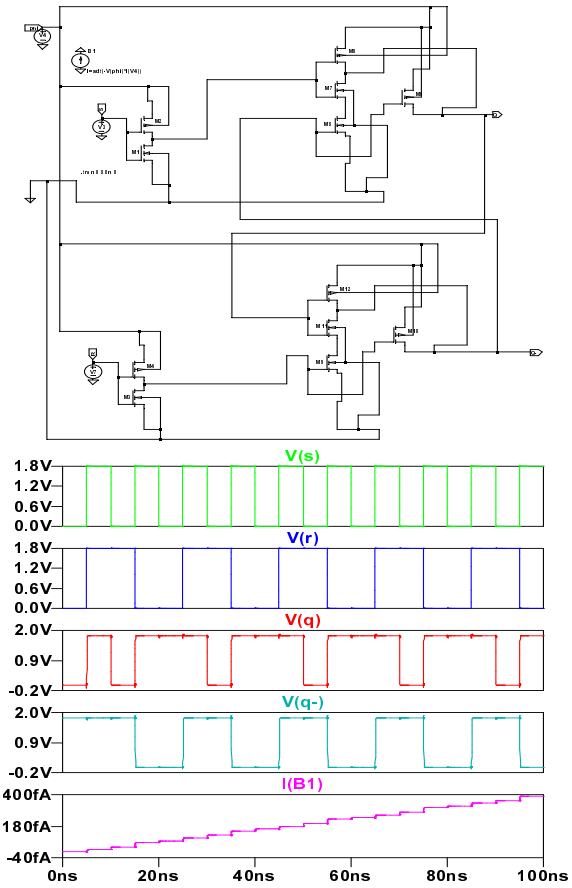

Fig. 3 Scheme and output waveforms of SR (set-reset) flip-flop of CMOS from the simulation.

Table 3 SR Flip-Flop operation (characteristic table)

Flip Flop	CMOS	2PASCL	Diff %
SR (at 100 MHz)	8.10 μ	2.24 μ	-72%
D (at 50 MHz)	5.32 μ	2.24 μ	-57.9 %

the SPICE simulation results, 2PASCL based flip-flops shown a significant lower energy dissipation compared to static CMOS based at 50 MHz for D flip-flop and 100 MHz for SR flip-flop.

References

[1] Wikipedia

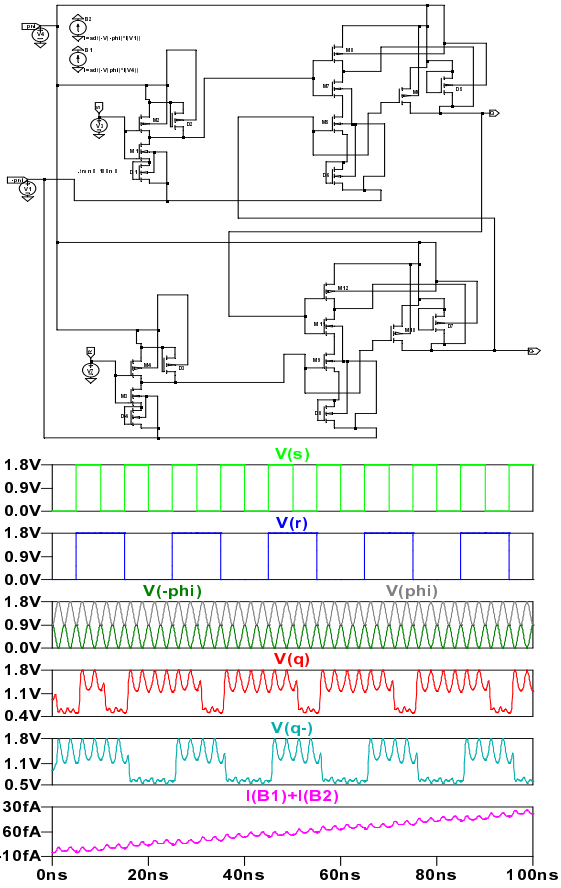

Fig. 4 Simulation output waveforms of SR (set-reset) flip-flop of 2PASCL.

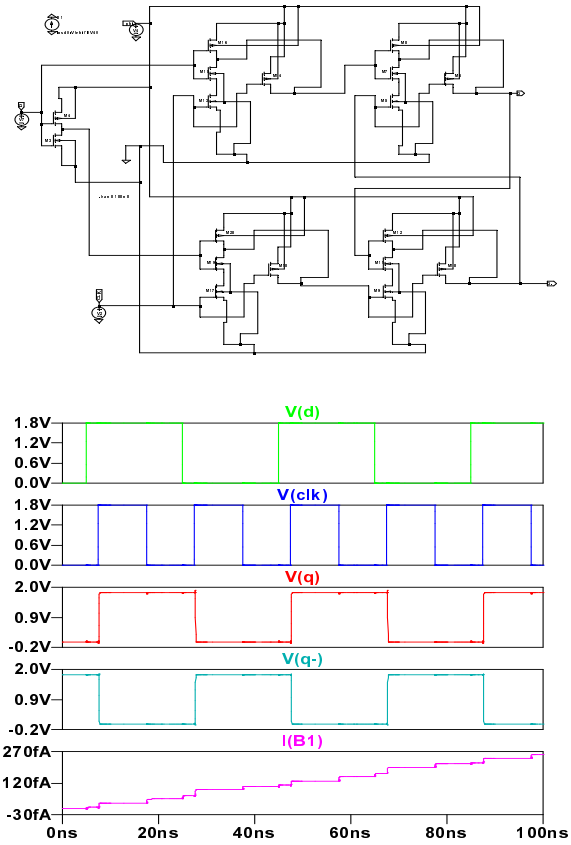

Fig. 5 Simulation output waveforms of clocked D (Data) flip-flop of CMOS.

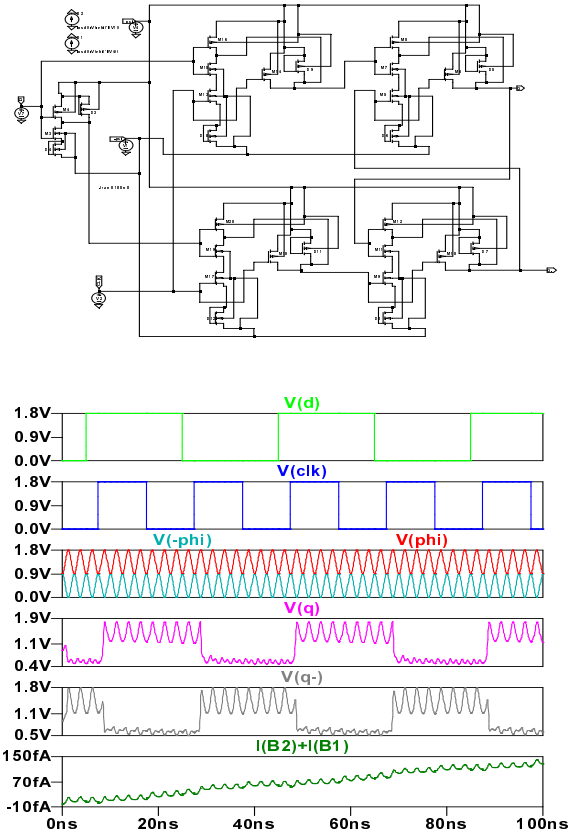

Fig. 6 Simulation output waveforms of clocked D (Data) flip-flop of 2PASCL.