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低電力断熱的論理回路のシミュレーションと消費エネルギーの比較

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あらまし　本論文は, 入力状態による消費エネルギーに着目して, 低電力断熱論理ゲートの設計法を調査する. 0.18 μm CMOS を用いて, インバータ回路を SPICE により回路シミュレーションを行う. 直流電圧 V_{dd} と等しい駆動パルス（波高）を論理ゲートに供給する. 消費エネルギーの特性を異なる負荷キャパシタンスの値においても比較する.
キーワード　低電力, 断熱論理, 負荷容量

Low-power Adiabatic Logic Circuit: Simulation and Energy Dissipation Comparison

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Abstract　This paper investigates the design approaches of low-power adiabatic logic gates in terms of energy dissipation associated with the input transition. A computer simulation using SPICE is carried out on several inverter circuits implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the logic gates. The dissipation characteristics are also compared at the different load capacitance values.
Key words　low-power, adiabatic logic, load capacitance

1. Introduction

CMOS has been the technology of choice for implementing low-power digital systems. It provides high density and high performance to the integrated circuits. As the density of an integrated circuit increases, the power consumption increases and it is difficult to control the temperature. A high performance, light weight, and long operation time required by mobile devices are just the contradictory characteristics. Adiabatic circuits, which are able to dissipate less energy than the fundamental limit of static CMOS, are promising candidates for low-power circuits in the frequency range in which signals are digitally processed. In recent years, studies on adiabatic computing have been utilized for low-power systems and several adiabatic logic families have been proposed [1]– [13].

In this paper we examine the functional and energy dissipation of adiabatic circuits using computer simulation whereas in [1], only functional simulations have been carried out. Then, we present a comparative study where the energy dissipation of the adiabatic circuits found in the literature are compared to that of conventional static CMOS circuit. We also simulate the effects of the load capacitance to the energy dissipation. We conclude with a discussion of directions for further research in adiabatic design.

1.1 Adiabatic Logic Circuit Group

The adiabatic circuits are classified into asymptotically adiabatic and quasi-adiabatic circuit based on whether full energy recovery or partial energy recovery is obtained.

1.1.1 Asymptotically Adiabatic Logic

Asymptotically adiabatic logic comprised of circuits in which dissipation results solely from finite rate of change of driving voltage and can be decreased to any desired levels. It is represented by 2n2p-2n logic [2], 1n1p logic that is using the split-level driving pulses [3] and split-level charge-recovery logic [4].

1.1.2 Quasi-Adiabatic Logic

Quasi-adiabatic logic [1] is comprised of circuits which dissipation can be reduced appreciably by lowering the rate of change of driving voltage. It is further divided into another two groups, which is the static approach and the dynamic approach. The static is represented by 1n-1p [5] and 2n-2n2p quasi-adiabatic logic [6], Adiabatic Dynamic Logic (ADL) [7] [8], Efficient Charge-Recovery Logic (ECRL) [9], Adiabatic Dynamic CMOS Logic (ADCL) [10], 2-Phase Adiabatic Dynamic CMOS Logic (2PADCL) [11] and 2n-2n2D [12]. The dynamic approach is represented by Hot-Clock nMOS (HCnMOS) logic [13].

2. Simulation and Results

2.1 Conditions

The paper starts by examining the functional and energy dissipation of a simple logic gate, an inverter. The following test methodology was utilized. The simulations using SPICE are carried out for all the inverters in this paper. The W/L of nMOS and pMOS logic gates used is 0.18 μm / 0.6 μm. Circuits are connected to the input signal X, according to the layouts. A capacitive load, C_L, of 0.01 pF is placed at each output node Y. The output loads are driven by clocked signals ϕ, which moves energy into and out of each gate. Using trapezoidal clocked driving voltage with 1.8 V peak-to-peak, the output waveforms at 50 MHz frequency are shown in Fig. 1 – Fig. 12, where the input signals are CMOS-compatible rectangular pulses.

The top graph shows the input signals. The second graph shows the pulse driving voltage. The third graph shows the output waveforms of a correctly functioning inverter and the bottom graph shows the energy dissipation of the logic gates which was simulated with the SPICE software. It can also be calculated by integrating the voltage and current product value as follows:

$$E = \int_0^{T_s} \left(\sum_{i=1}^{n} (V_{pi} \times I_{pi}) \right) dt, \qquad (1)$$

where T_s is the period of the primary input signal, V_p is the power supply voltage, I_p is the power supply current and i is the number of power supply [11].

2.2 Circuits comparison

Table 1 lists the features of all logics in the review for comparison. In this preliminary results, ADL gives the lowest value of dissipated energy per cycle while 2n-2n2p quasi adiabatic shows the highest. 8 out of 11 adiabatic circuits show a lower energy dissipation compared to conventional static CMOS by reducing it from 98% to 17%.

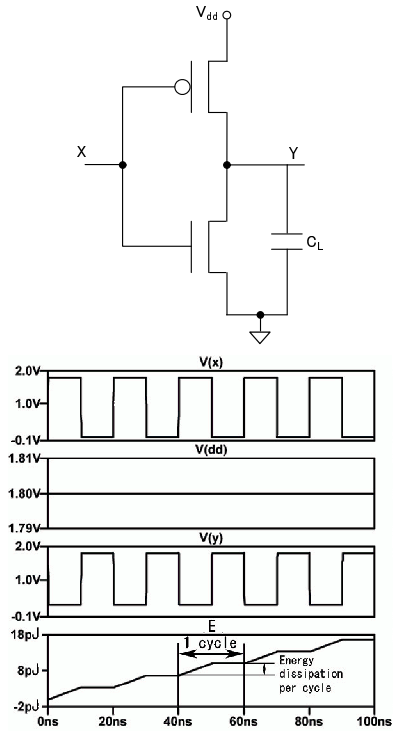

図 1　従来の CMOS インバータ回路と波形

Fig. 1　Conventional CMOS logic inverter circuit diagram and waveforms

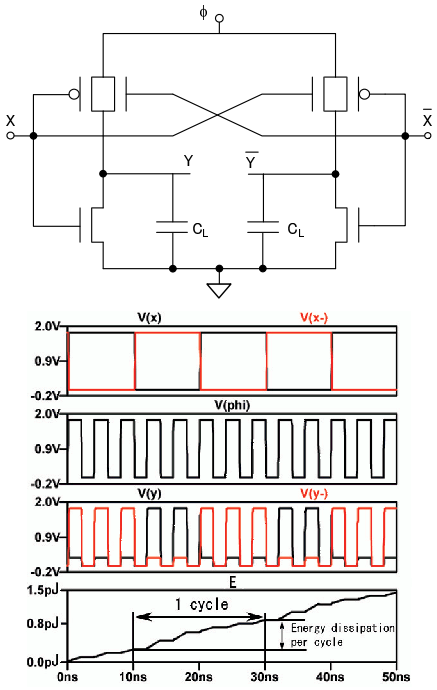

図 2　2n2p-2n インバータ回路と波形

Fig. 2　2n2p-2n adiabatic logic inverter circuit diagram and waveforms

2.3 Energy dissipation at different load capacitance

The simulation result on the energy dissipation at different load capacitance, C_L is shown in Fig. 13. As expected, all the circuits, except 2PADCL, show an increase of dissipated

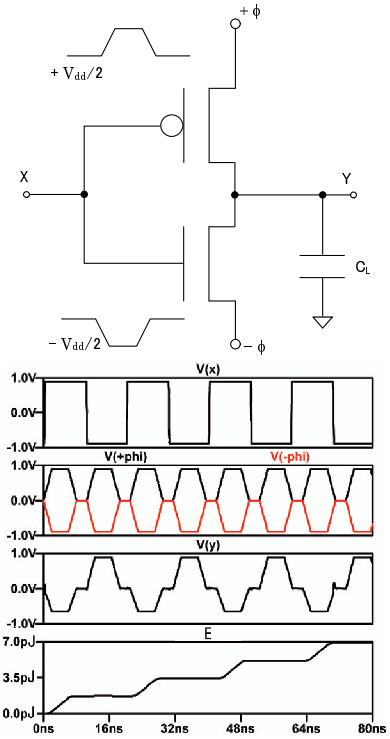

図 3　スプリットレベルパルス　1n1p インバータ回路と波形

Fig. 3　Split level pulse 1n1p logic inverter circuit diagram and waveforms

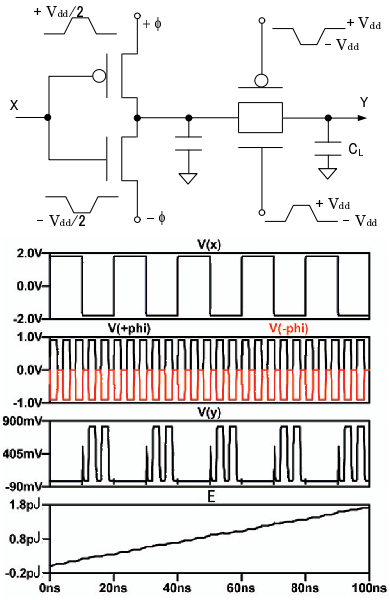

図 4　スプリットレベルチャージリカバリ インバータ回路と波形

Fig. 4　Split level charge-recovery logic inverter circuit diagram and waveforms

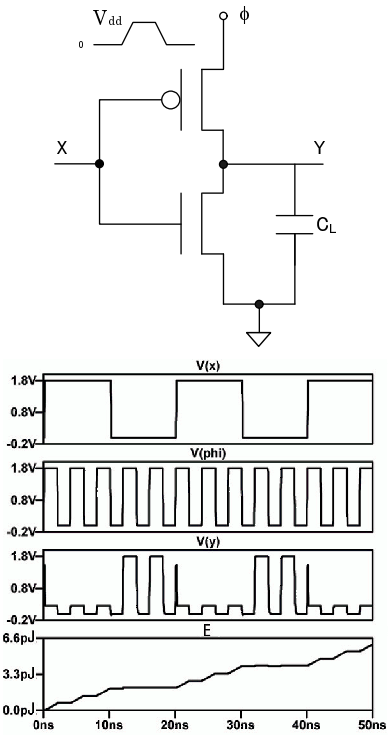

図 5　1n-1p インバータ回路と波形

Fig. 5　1n-1p quasi-adiabatic logic inverter circuit diagram and waveforms

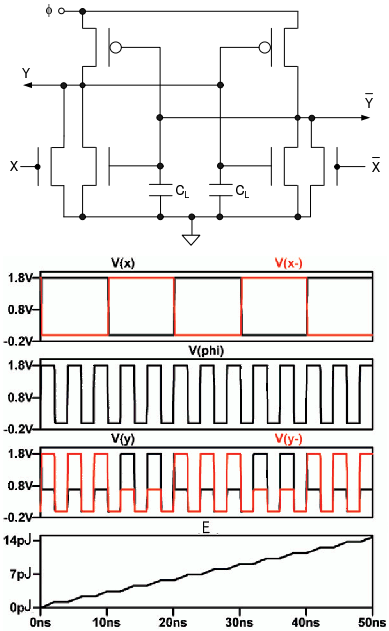

図 6　2n-2n2p インバータ回路と波形

Fig. 6　2n-2n2p quasi-adiabatic logic inverter circuit diagram and waveforms

energy when changing the load capacitor to a higher value.

3. Discussion

Analysis of the adiabatic circuits using SPICE shows that the energy dissipation per cycle can be calculated and therefore is convenient for futher analysis and design. In this simulation result, ADL shows the lowest energy dissipation as an inverter. However, since ADL which uses 4-phase driving pulse, whereas 2n-2n2D and ADCL, both uses only 1-phase driving pulse voltage is better. ADCL, which uses 4 gates instead of 6 gates used in the 2n-2n2D is the most suitable from this simulation results for an adiabatic inverter logic circuit. From table 1, diode based adiabatic inverters demonstrate a

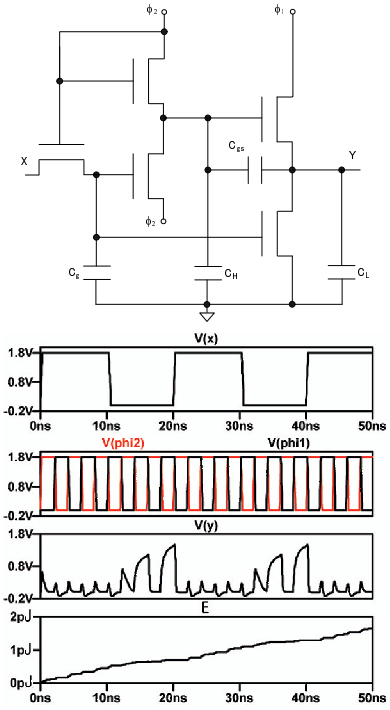

図 7　HCnMOS インバータ回路と波形

Fig. 7　Hot-clock nMOS logic inverter circuit diagram and waveforms

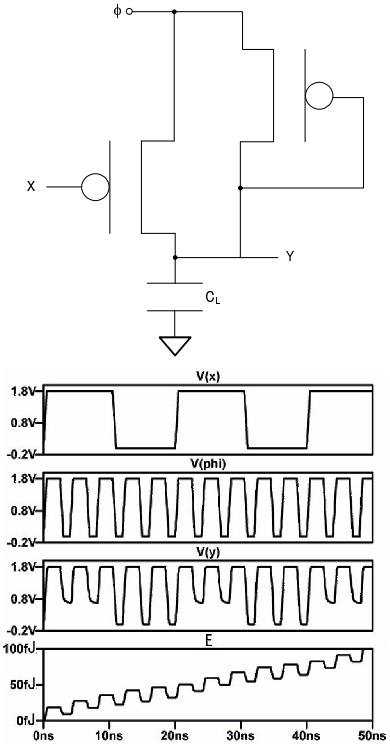

図 8　ADL インバータ回路と波形

Fig. 8　Adiabatic Dynamic logic (ADL) inverter circuit diagram and waveforms

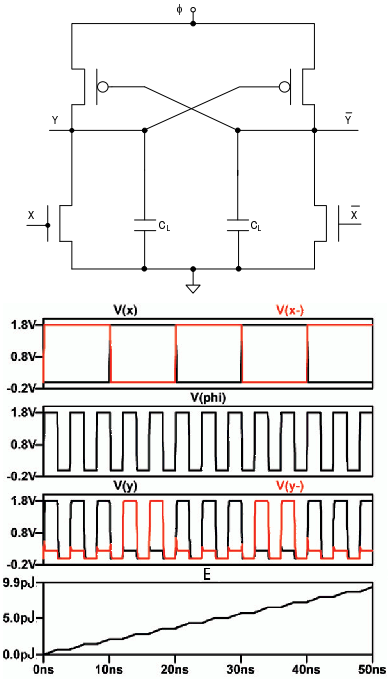

図 9　ECRL インバータ回路と波形

Fig. 9　Efficient charge-recovery logic (ECRL) circuit diagram and waveforms

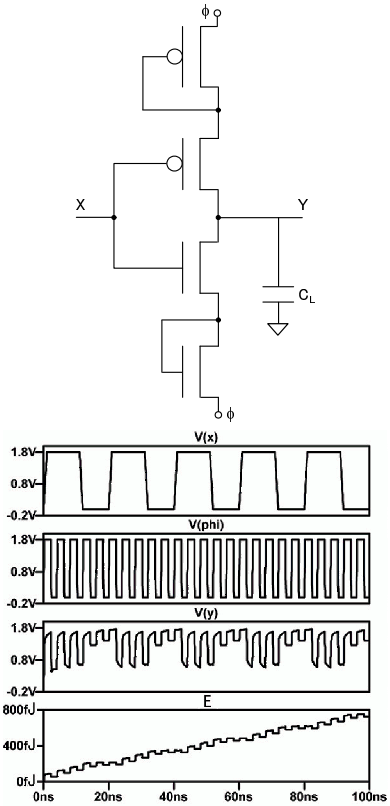

図 10　ADCL インバータ回路と波形

Fig. 10　Adiabatic Dynamic CMOS logic (ADCL) circuit diagram and waveforms

good result which reduced 98% to 77% of the conventional CMOS logic inverter energy dissipation. Diodes in the adiabatic circuit are used for charging and recycling the charge from the output. Load capacitance which is used as the data holder needs to be designed precisely considering the time constant that affect the output signal and also the amount of information to be stored. Unlike other circuits, 2PADCL

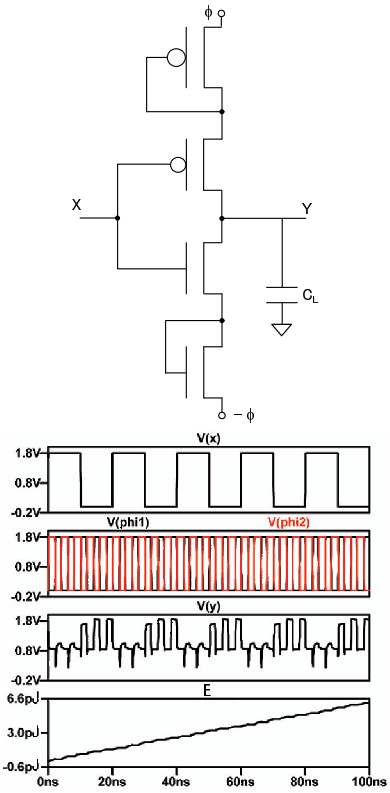

図 11　2PADCL インバータ回路と波形

Fig. 11　Two-phase drive adiabatic dynamic CMOS logic (2PADCL) circuit diagram and waveforms

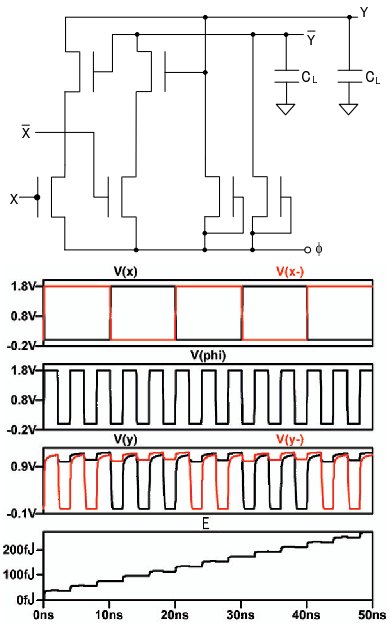

図 12　2n-2n2D インバータ回路と波形

Fig. 12　2n-2n2D circuit diagram and waveforms

shows a decrease in energy dissipation when the load capacitance increased. If this is true, this circuit has a higher possibility to be further studied.

4. Conclusion

We have done simulations to find out the functional and energy dissipation characteristic of each adiabatic logic circuits. The SPICE simulations using trapezoidal power clock prove that the designed circuits have the correct logic function and considerable energy saving. The design principle can also be used for designing more complicated adiabatic CMOS circuits. We conclude that most of the proposed circuits have lower energy dissipation compared to conventional CMOS logic.

表 1　消費エネルギーの比較

Table 1　Comparison of Energy Dissipation

Adiabatic Logic	Energy(pJ/cycle)	Gates	Driving Pulse
ADL	0.035	4	4
2n-2n2D	0.095	6	1
ADCL	0.133	4	1
1n-1p SLCR	0.34	4	1
HCnMOS	0.60	5	2
2PADCL	0.77	4	2
1n-1p SLP	0.86	2	2
1n-1p quasi	2.04	2	1
CMOS	3.33	2	1
2n2p-2n	3.45	6	1
ECRL	3.61	4	1
2n-2n2p quasi	5.69	6	1

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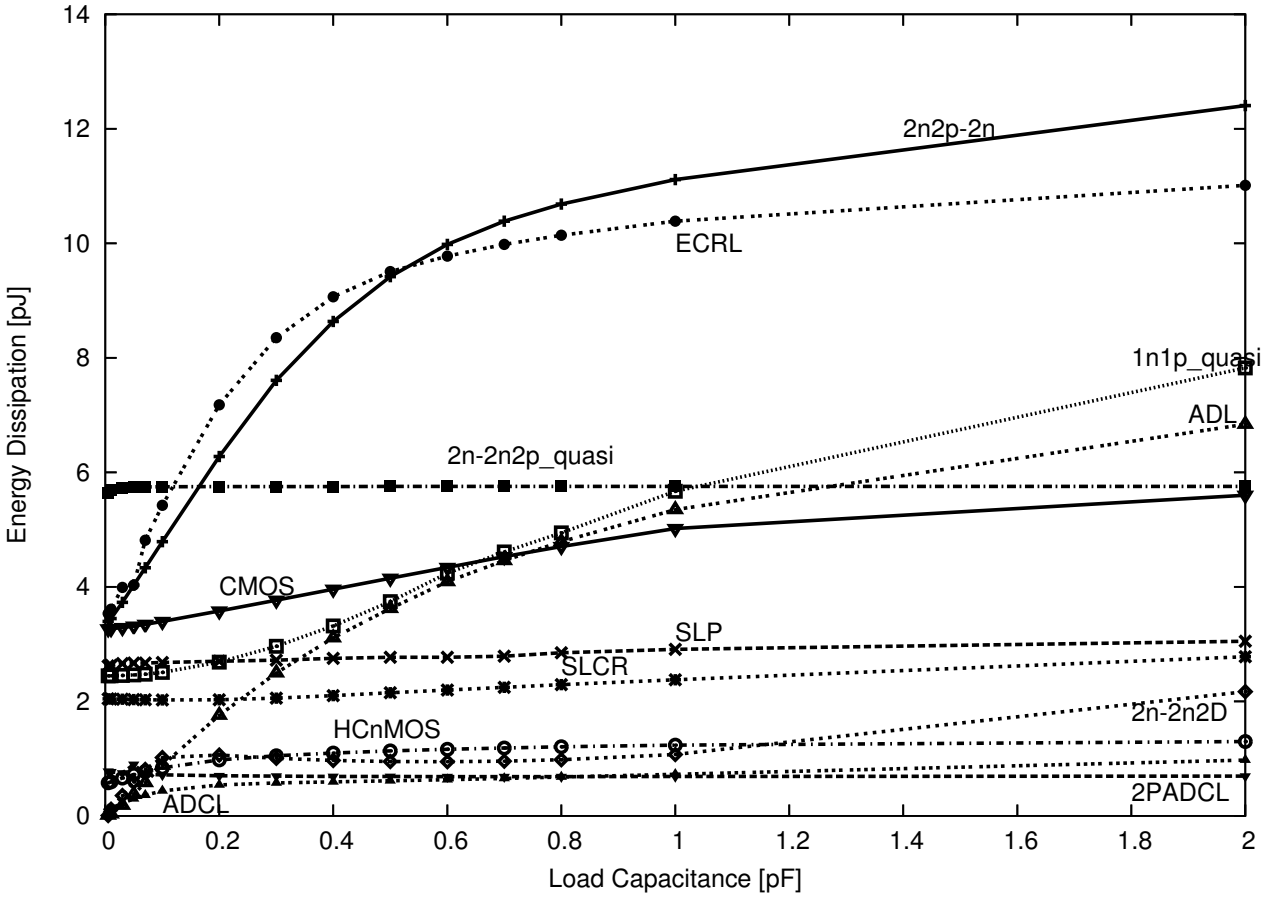

図 13　負荷容量による消費エネルギーの変化の比較

Fig. 13　Energy dissipation comparison in adiabatic circuits at different load capacitance value

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