2PASCL: Energy dissipation of NAND circuit using trapezoidal and split level pulse driving and the effects of rise and fall time

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Abstract

This paper proposes a new quasi adiabatic logic family that uses two complementary pulsed supply clock for digital low power applications such as sensors. The proposed two-phase adiabatic static CMOS logic circuit (2PASCL) has switching activity that is lower than dynamic logic and can be directly derived from static CMOS circuits. We have done a SPICE simulation on the 2PASCL NAND implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the gates. This circuit is emphasis on the recycle of the charges as two diodes are placed for the discharging. The ealier results show that 2PASCL can save a maximum of 63.3% of power dissipation over static CMOS logic at transition frequencies of 50MHz to 100MHz.

1 Introduction

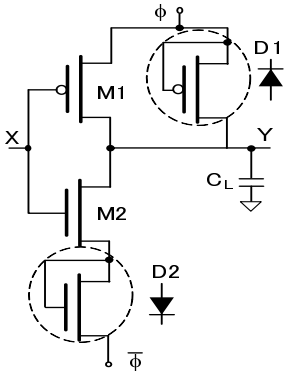
In the previous simulation, we have confirmed the functional of 2PASCL as NAND logic circuit. However, the energy dissipation of 2PASCL NAND is higher than static CMOS at 10 MHz transition frequency. In terms of clocking voltage driving, trapezoidal waveforms showed a lower energy dissipation compared to pulse and sinusoidal waveforms. We also found that the high and low output signal cannot be separated in two inverted phase driving.

In this simulation, we are going to examine the effects of rise and fall time of the trapezoidal to the energy dissipation. We will use split level pulse driving in this simulation to avoid the mixed output signal. The simulation to compare the energy dissipation of the trapezoidal, split level pulse driving and static CMOS NAND will be carried out. The 2PASCL circuit diagram and its truth table are shown in Fig. 1.

2 Simulation and results

The simulation of 2PASCL NAND circuit as in schematic diagram shown in Fig. 2 has been done. The differences compared to static CMOS NAND circuit are two diodes placed near the output and next to the nMOS logic and clocking voltage power supply to replace the V_{dd} and the ground. Its function is evaluated using the output waveforms graph. Then by using the SPICE simulation, the energy dissipation for one cycle is calculated. The energy in joule is then converted to watt by multiplying it with the input frequency.

For the simulation in this paper, the V_{dd} is scaled to 1.2V. The diode W/L is 0.6μm/0.18μm. At circuit condition shown in Fig.1, energy dissipation per cycle of 50 MHz and 100 MHz is compared at different rise and fall time of the trapezoidal driving pulse. From the result in Table 3, we understand that the higher the rise and fall time, the lower the energy dissipation will be.



X	ϕ	Y
$1 \longrightarrow 0$	$V_\phi \rightarrow$ Hi	V_ϕ
	$V_\phi \rightarrow$ Lo	V_ϕ
$0 \longrightarrow 1$	$V_{\overline{\phi}} \rightarrow$ Hi	V_t
	$V_{\overline{\phi}} \rightarrow$ Lo	V_t

Fig. 1 2PASCL inverter circuit and its truth table

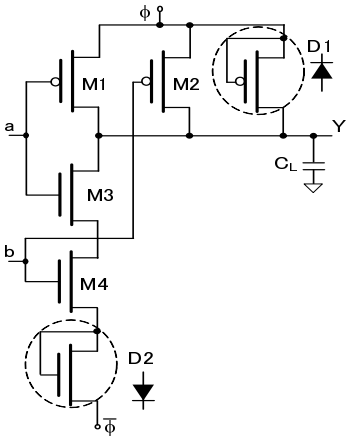


Fig. 2 NAND logic circuit with 2PASCL configuration.

The consequent simulation is using the two phase inverted and the split level driving pulse. By comparison the output waveform, we can easily differentiate the Lo and Hi signal output by using the split level driving pulse as shown in Fig. 4 compared to Fig. 5

Next, by using the T_{rise}, T_{fall} of 0.6n of split level pulse, which is the maximum value of T_{rise} , T_{fall} for 100 MHz input we simulate at the transition frequency of 10 to 100 MHz and compared the result with CMOS NAND circuit at the same frequencies. We also com-

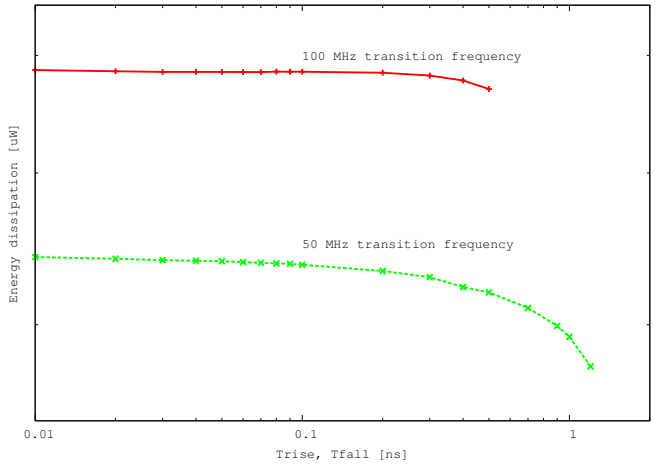


Fig. 3 NAND logic circuit with 2PASCL configuration.

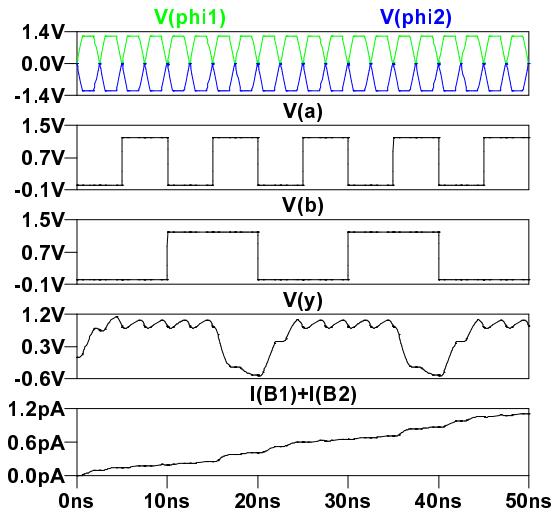


Fig. 4 NAND logic circuit with split level.

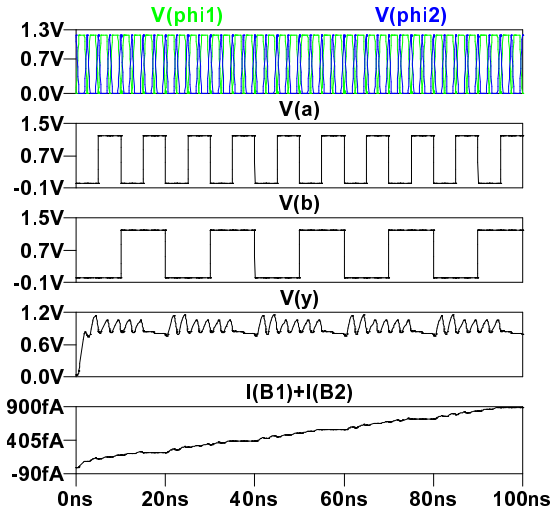


Fig. 5 NAND logic circuit with 2 phase inverted.

pared the result with two phase inverted and the split level driving at the best condition. The best condition here is the by taking a minimum driving pulse frequency which is four times the input frequency and the maximum T_{rise} , T_{fall}. The result is demonstrated in Fig. 6. From the result, we understand the 2PASCL still need further investigation as the energy dissipation is higher compared to CMOS.

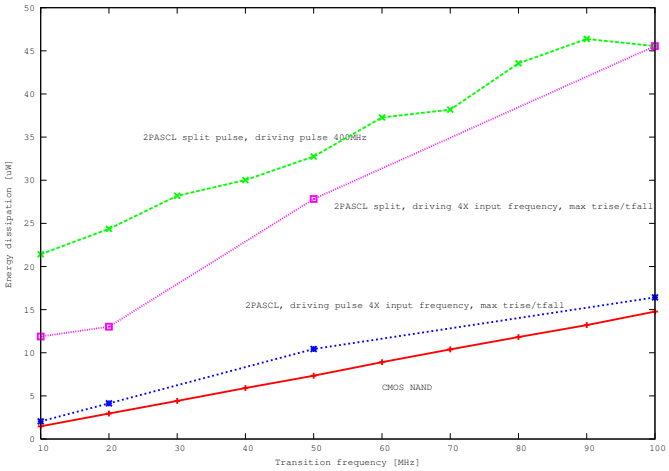


Fig. 6 NAND logic circuit with 2PASCL configuration.

Table 1 Input signal for T_{rise} and T_{fall} simulation

Input a	pulse, T_{on}: 20n(50MHz),10n(100MHz)
Input b	pulse, T_{on}: 40n(50MHz),20n(100MHz)
C_L	0.1 pF
Diodes	W/L : 0.6μm/0.18μm
nMOS, pMOS	W/L : 0.6μm/0.18μm

Clocking voltage power condition

- Trapezoidal at 100 MHz
  - ϕ V_{init}=0V, V_{on}=1.2V, delay=0n, T_{rise}/T_{fall}=0.01$\sim$ 0.5n, T_{on}=1.25n, T_{period}=2.5n
  - $\overline{\phi}$ V_{init}= 1.2V,V_{on}=0V, delay=0n, T_{rise}/T_{fall}=0.01$\sim$ 0.5n, T_{on}=1.25n, T_{period}=2.5n
- Trapezoidal at 50 MHz
  - ϕ V_{init}=0V, V_{on}=1.2V, delay=0n, T_{rise}/T_{fall}=0.01$\sim$ 1.2n, T_{on}=2.5n, T_{period}=5n
  - $\overline{\phi}$ V_{init}= 1.2V,V_{on}=0V, delay=0n, T_{rise}/T_{fall}=0.01$\sim$ 1.2n, T_{on}=2.5n, T_{period}=5n

3 Conclusion

From this simulation, the functional of 2PASCL as NAND logic circuit has been confirmed by using split level driving compared to 2 phase inverted pulse. Split lvel driving produced better output waveforms which differentiate clearly the Hi and Lo signal. However the energy dissipation is higher when using split level pulse. We also did a simulation on the T_{rise}, T_{fall} and clearly the slower the rise and the fall time, the lower energy dissipation. 2PASCL still need a further study as the energy dissipation at frequency of 10 to 100 MHz is still higher compared to CMOS.