PAPER

Adiabatic Circuits Simulation and Energy Dissipation Comparison at different load capacitance

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SUMMARY The current status of research and development in the field of adiabatic electronic devices for the production of information is reviewed. An adiabatic logic is a technique to design low power digital VLSI. In this presentation, several computer simulations using LTSpice have been carried out on the circuits in [1] and the total energy dissipation at different load capacitance are compared.

key words: *adiabatic logic*

Presentation content

- 2008/09/26 : Circuit Simulation and Energy dissipation at different C
- 2008/10/03 : Circuit Simulation and Energy dissipation at different C (continue)

1. Introduction

1.1 Adiabatic Logic Circuit Group

1.1.1 Asymptotically Adiabatic Logic

In [1], asymtotically adiabatic logic comprised of circuits in which dissipation results solely from finite rate of change of driving voltage and can be decreased to any desired level. In [1], it is represented by 2n2p-2n logic, 1n1p logic that is using the split-level driving pulses and split-level charge-recovery logic. All the examples are the inverter circuits.

1.1.2 Quasi-Adiabatic Logic

In [1], quasi-adiabatic logic comprised of circuits which dissipation can be reduced appreciably by lowering the rate of change of driving voltage.It is divided into another 2 groups, which is the static approach and the dynamic approach. The static is represented by 1n-1p quasi-adiabatic logic and 2n-2n2p quasi-adiabatic logic. While the dynamic approach is represented by Hot-clock nMOS (HCnMOS) logic, recovered-energy logic (REL), Adiabatic Dynamic Logic (ADL) and Efficient charge-recovery logic (ECRL). These logic examples are also given as inverter circuits.

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2. Simulation and Results

2.1 Conditions

Computer simulations using LTSpice are carried out for all the inverter circuits in [1]. Circuits are connected to the pulse driving voltage and input signal according to the diagrams. Depending on the circuits, the input pulse T (time for 1 cycle) supplied ranging from 20 ns to 55 ns. Length and width of the nMOS and pMOS gates used in this simulation are L=0.18 μm, W=0.6 μm. The most suitable load capacitor value for each circuits is examined according to the output voltage waveforms. Circuits diagrams and simulation results in the form of waveforms are represented by Fig. 1 $\sim$ Fig. 10

2.2 Circuits comparison

Table 1 lists the features of all logics in the review for comparison

2.3 Energy dissipation at different load capacitance

The simulation result on the energy dissipation at different load capacitance is shown in Fig. 11.

3. Conclusion

- Analysis of the adiabatic circuits using LTSpice shown that the energy dissipation can be calculated and therefore is convinience for futher analysis and design.
- Load Capacitance which use as the data holder need to be design precisely considering the time constant that effect the output and also the amount of information to be stored

References

[1] V.I Starosel'skii : Russian Microelectronics, 2002, Vol.31, No. 1, pp.37-58

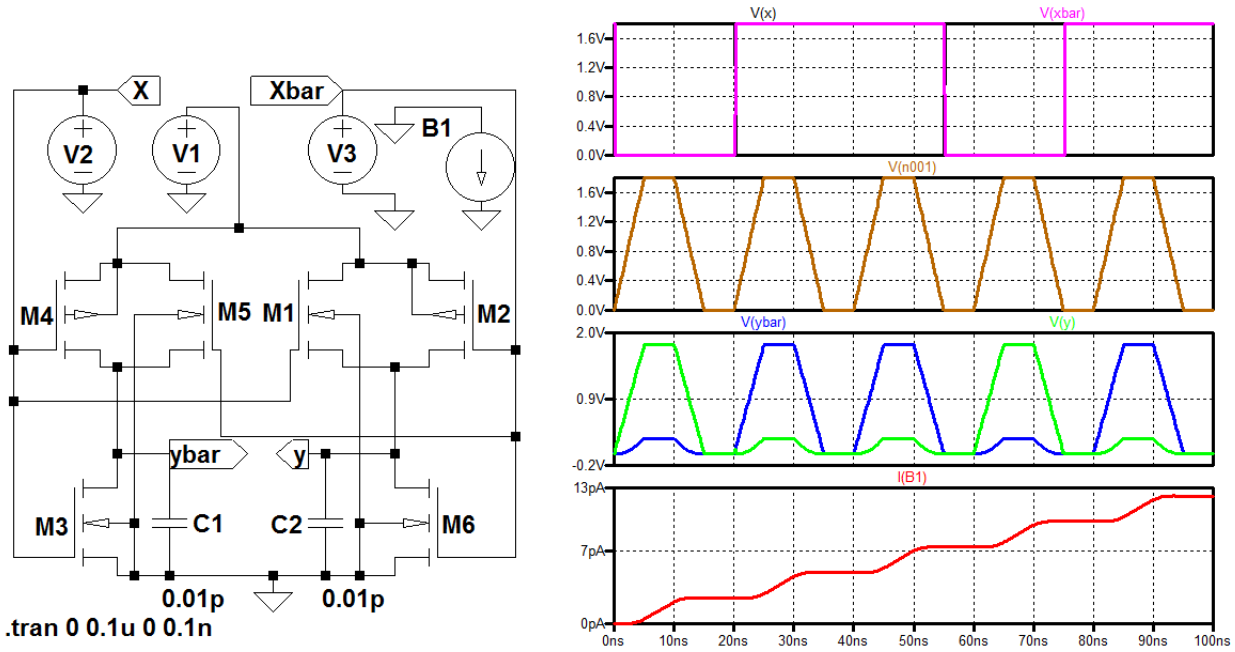

Fig. 1 2n2p-2n adiabatic logic inverter circuits diagram and waveforms

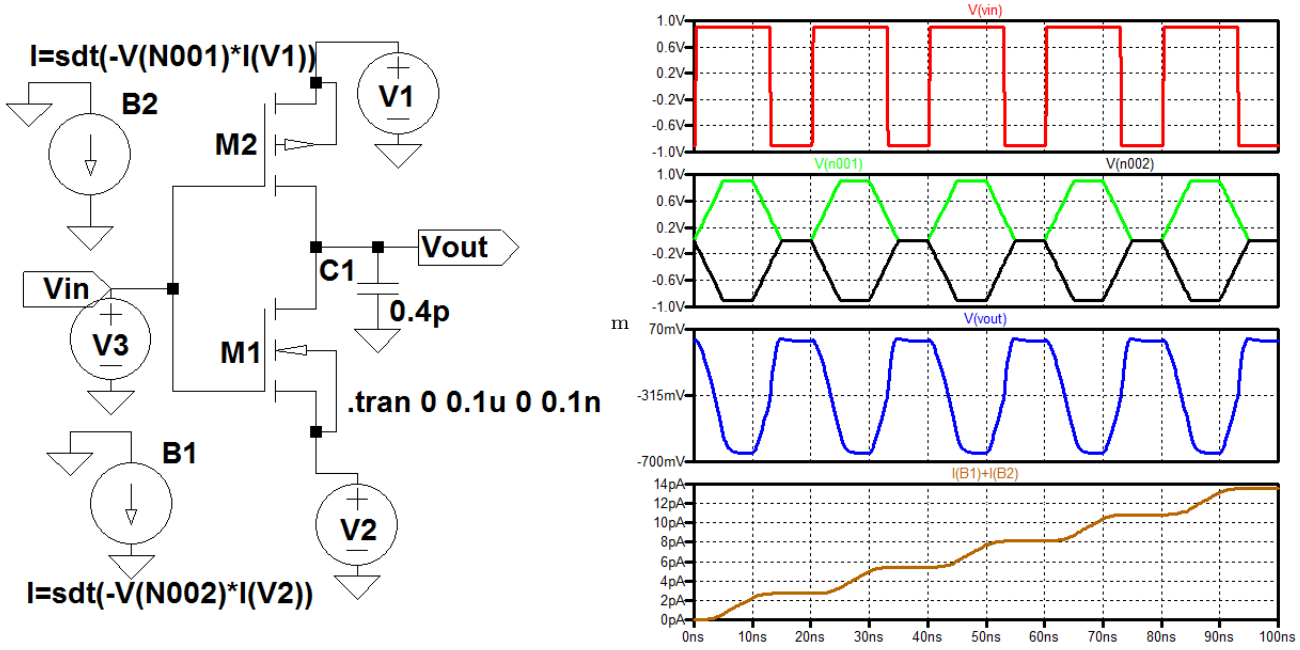

Fig. 2 Split level pulse 1n1p logic inverter circuits diagram and waveforms

Table 1 Comparison of Power Dissipation

	2n2p-2n	1n-1p SLP	1n1p SLCR	1n-1p	2n-2n2p	HCnMOS	REL	REL MOS	ADL	ECRL
Ener. diss.(pJ/cyc)	5.72	2.71	0.53	2.45	11.31	0.087	4009.28	672.88	LARGE	1.28
Number of gates	6	2	4	2	6	5	4	4	4	4
Driving pulse	1	2	1	1	1	2	1	1	4	1

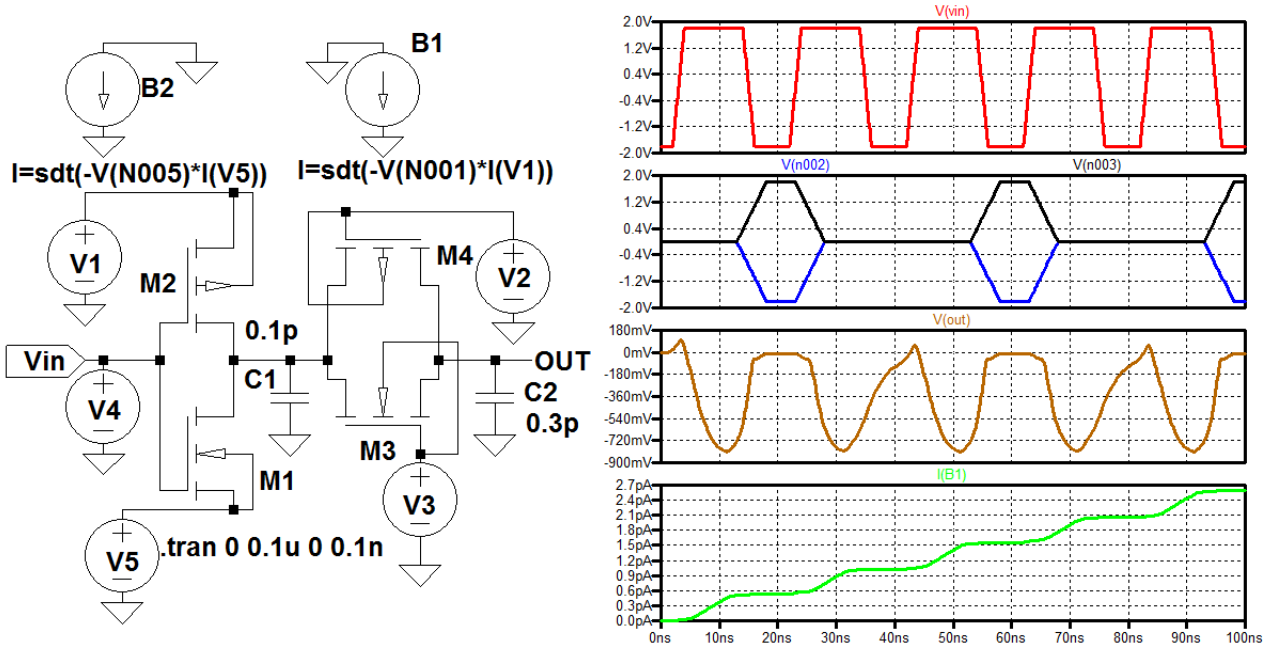

Fig. 3 Split level charge-recovery logic inverter circuits diagram and waveforms

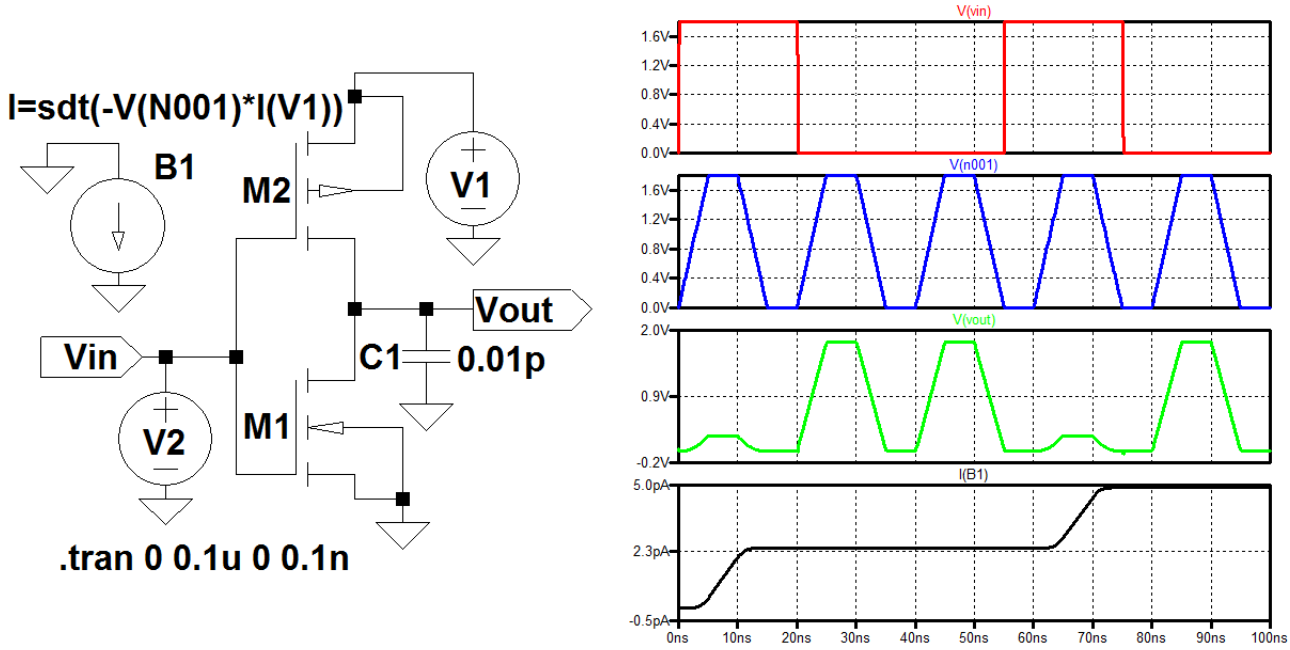

Fig. 4 1n-1p quasi-adiabatic logic inverter circuits diagram and waveforms

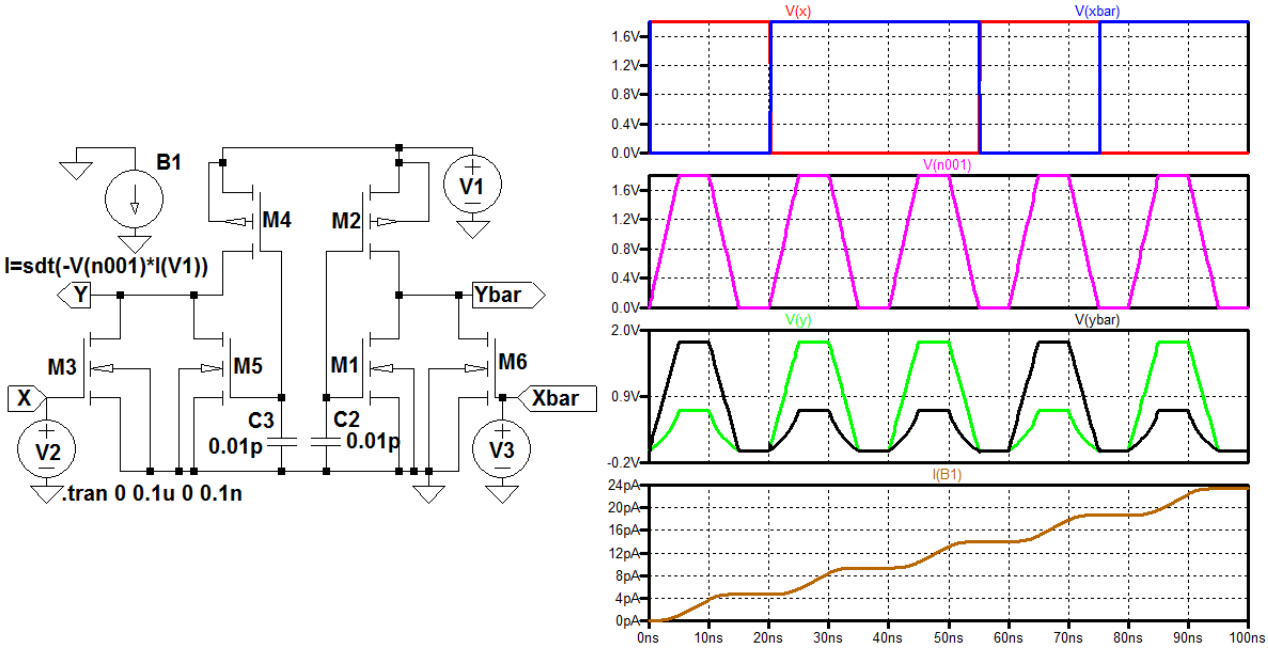

Fig. 5 2n-2n2p quasi-adiabatic logic inverter circuits diagram and waveforms

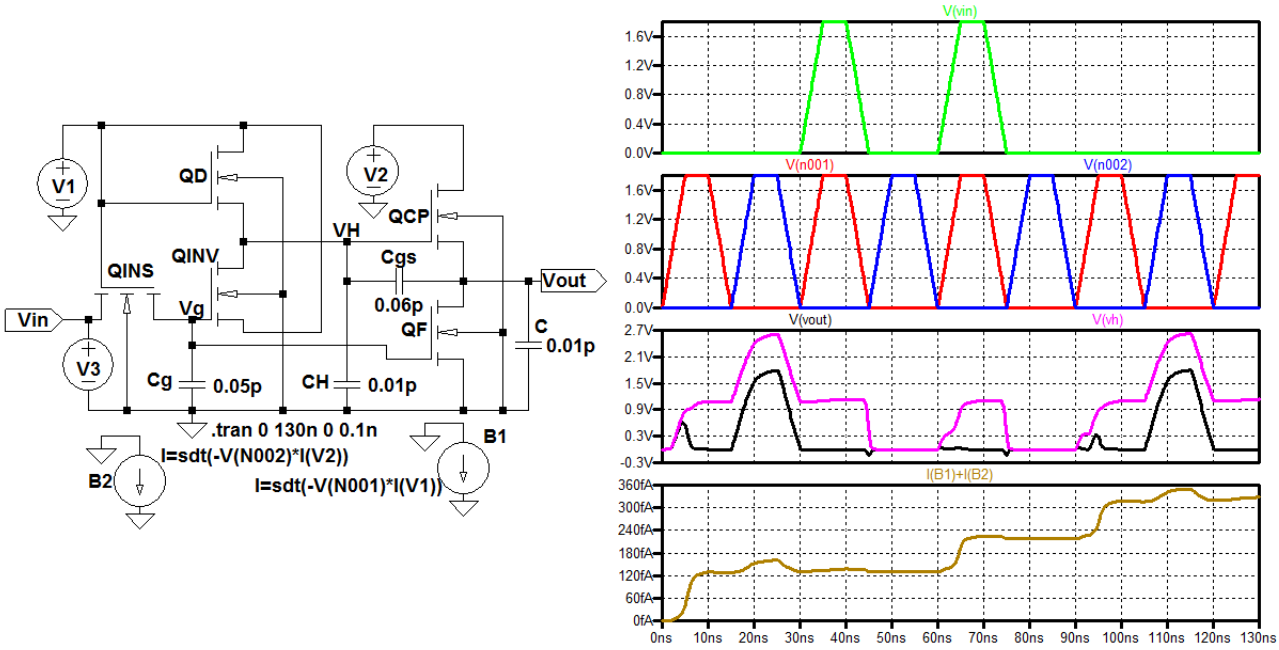

Fig. 6 Hot-clock nMOS logic inverter circuits diagram and waveforms

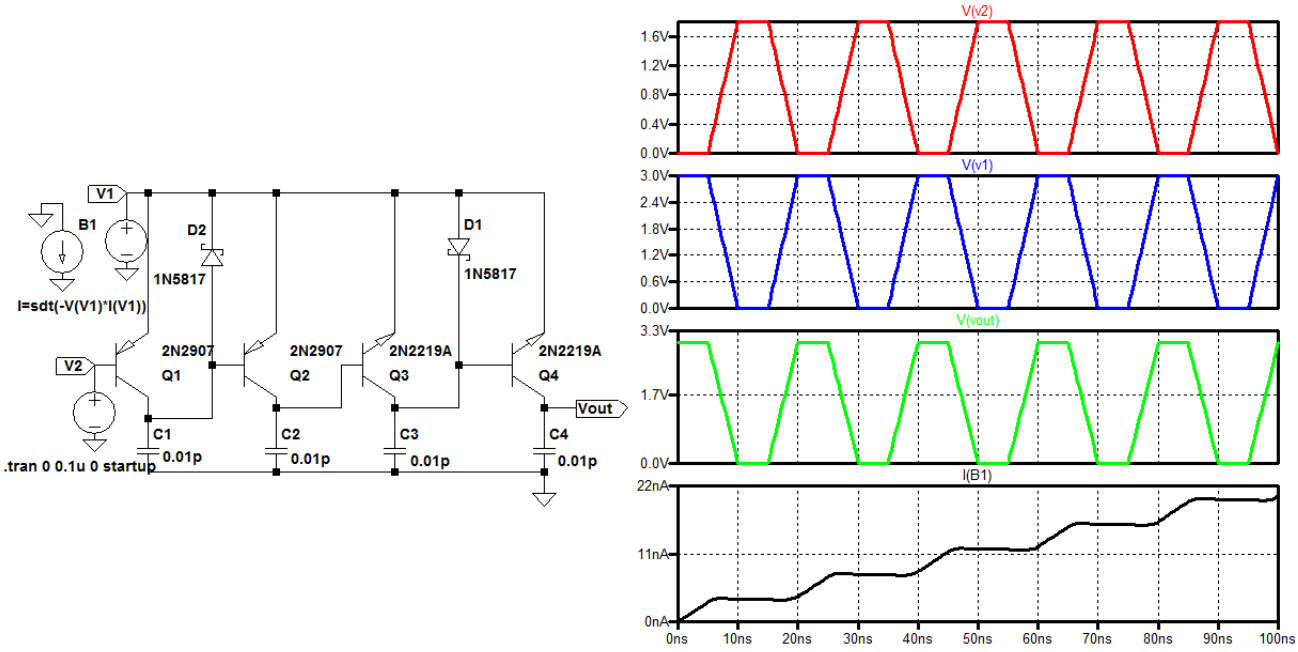

Fig. 7 Recovered-energy logic (REL) inverter circuits diagram and waveforms

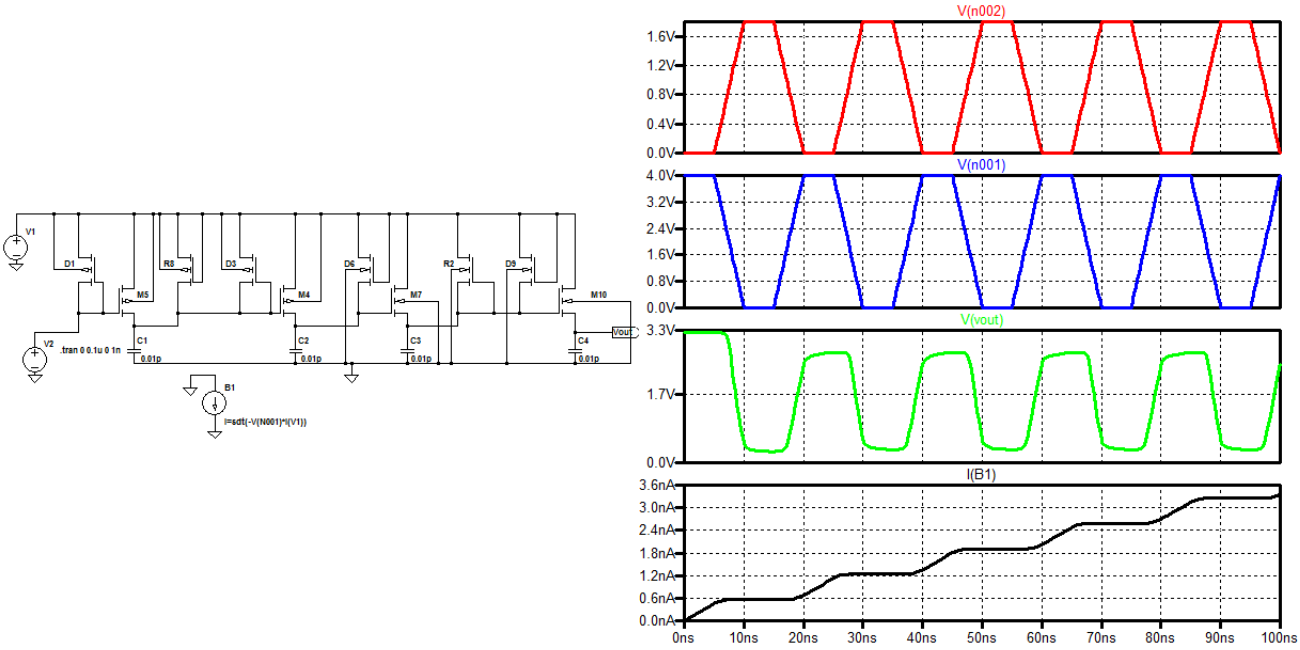

Fig. 8 Recovered-energy logic (REL) in MOSFETs inverter circuits diagram and waveforms

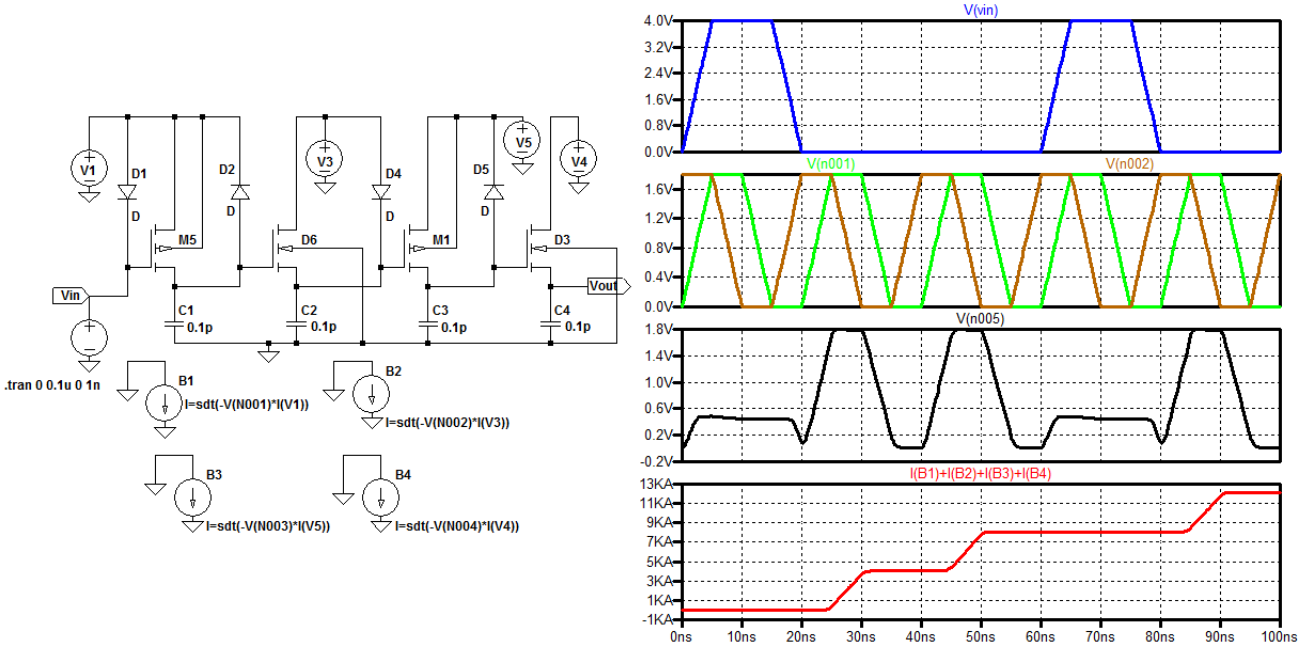

Fig. 9 Adiabatic Dynamic logic (ADL) inverter circuits diagram and waveforms

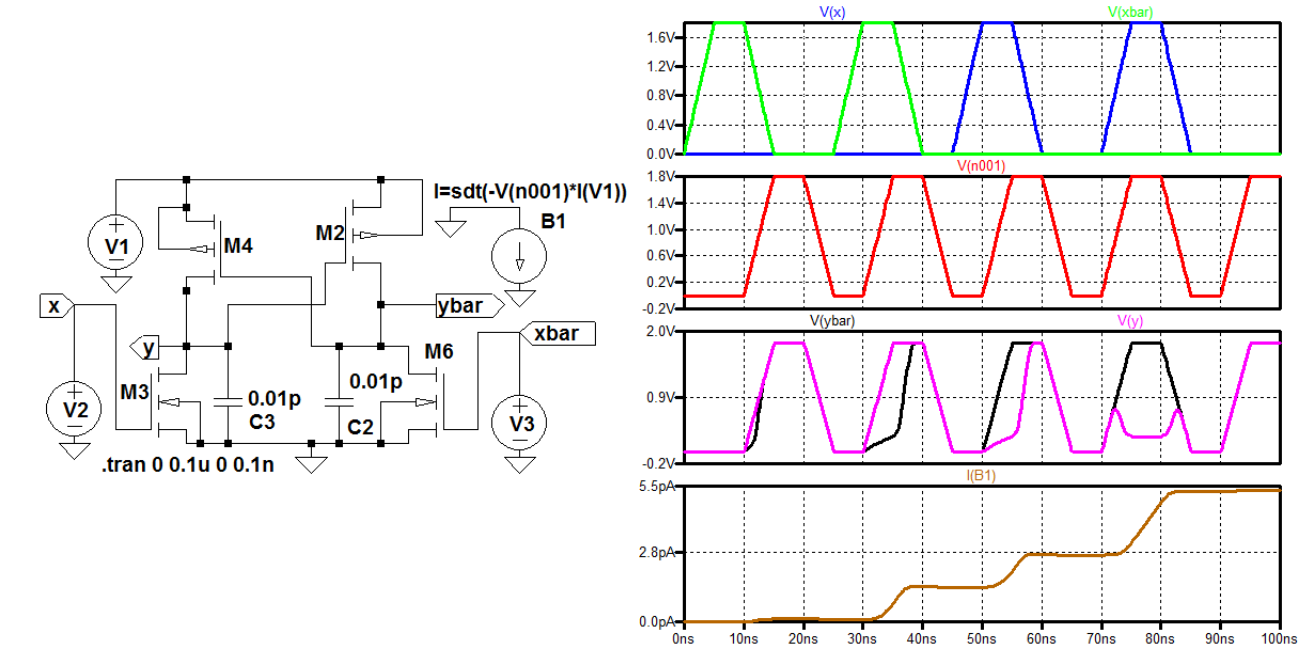

Fig. 10 Efficient charge-recovery logic (ECRL) circuits diagram and waveforms

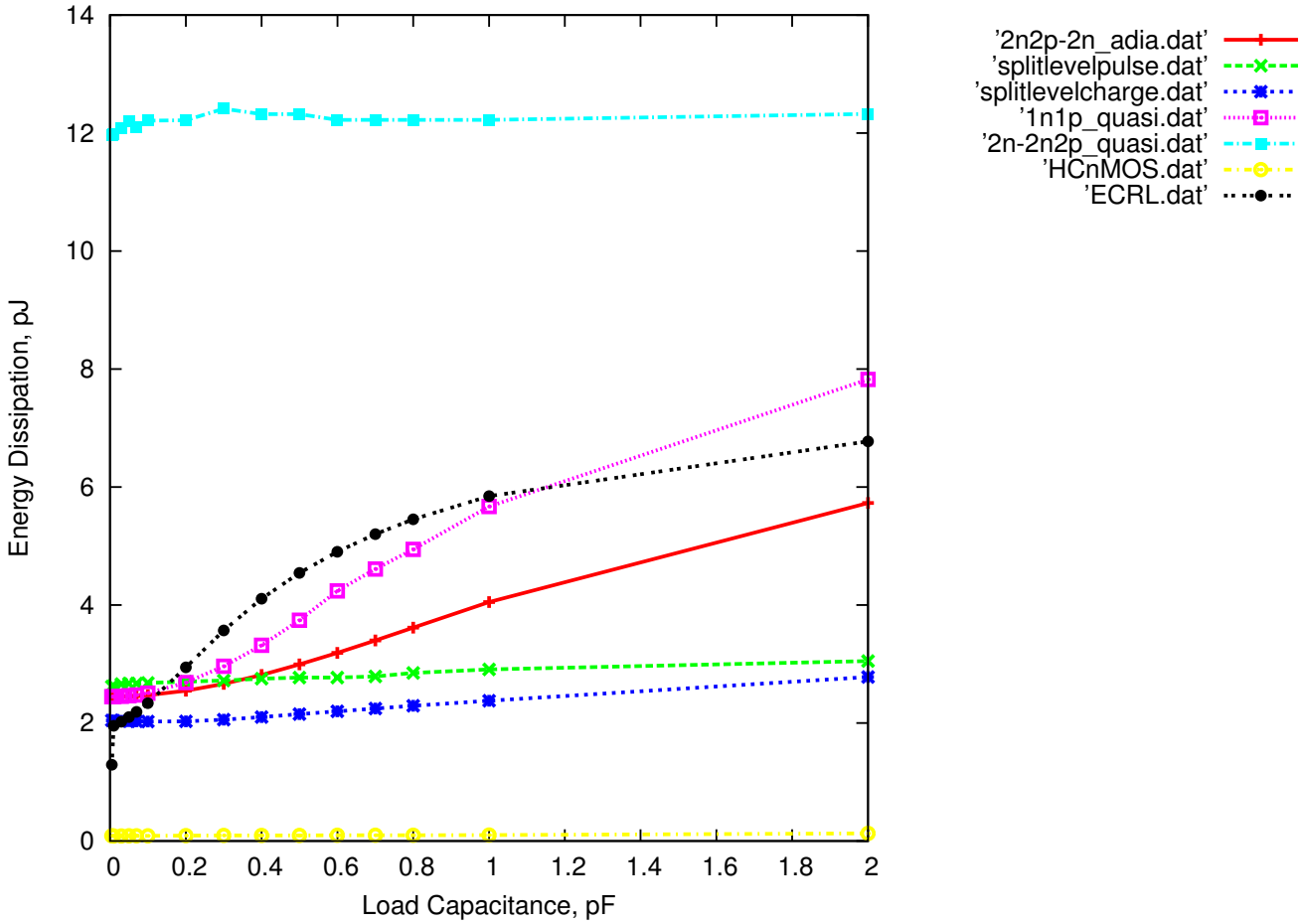

Fig. 11 Energy dissipation comparison in adiabatic circuits at different load capacitance value