PAPER

Adiabatic Circuits Simulation and Energy Dissipation Comparison at different load capacitance

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SUMMARY The current status of research and development in the field of adiabatic electronic devices for the production of information is reviewed. An adiabatic logic is a technique to design low power digital VLSI. In this presentation computer simulations using LTSpice have been carried out on the circuits in [1] and the total power dissipations at different load capacitance values are compared.

key words: *adiabatic logic*

1. Adiabatic Logic Circuit Group

1.1 Asymptotically Adiabatic Logic

In [1], asymtotically adiabatic logic comprised of circuits in which dissipation results solely from finite rate of change of driving voltage and can be decreased to any desired level. In [1], it is represented by 2n2p-2n logic, 1n1p logic that is using the split-level driving pulses and split-level charge-recovery logic. All the examples are the inverter circuits.

1.2 Quasi-Adiabatic Logic

In [1], quasi-adiabatic logic comprised of circuits which dissipation can be reduced appreciably by lowering the rate of change of driving voltage.It is divided into another 2 groups, which is the static approach and the dynamic approach. The static is represented by 1n-1p quasi-adiabatic logic and 2n-2n2p quasi-adiabatic logic. While the dynamic approach is represented by Hot-clock nMOS (HCnMOS) logic, recovered-energy logic (REL), Adiabatic Dynamic Logic (ADL) and Efficient charge-recovery logic (ECRL). These logic examples are also given as inverter circuits.

2. Conclusion

1. Analysis of the adiabatic circuits using LTSpice shown that the energy dissipation can be calculated and therefore is convinience for futher analysis and design.

2. Load Capacitance which use as the data holder need to be design precisely considering the time constant that effect the output and also the amount of information to be stored.

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References

[1] V.I Starosel'skii : Russian Microelectronics, 2002, Vol.31, No. 1,pp.37-58

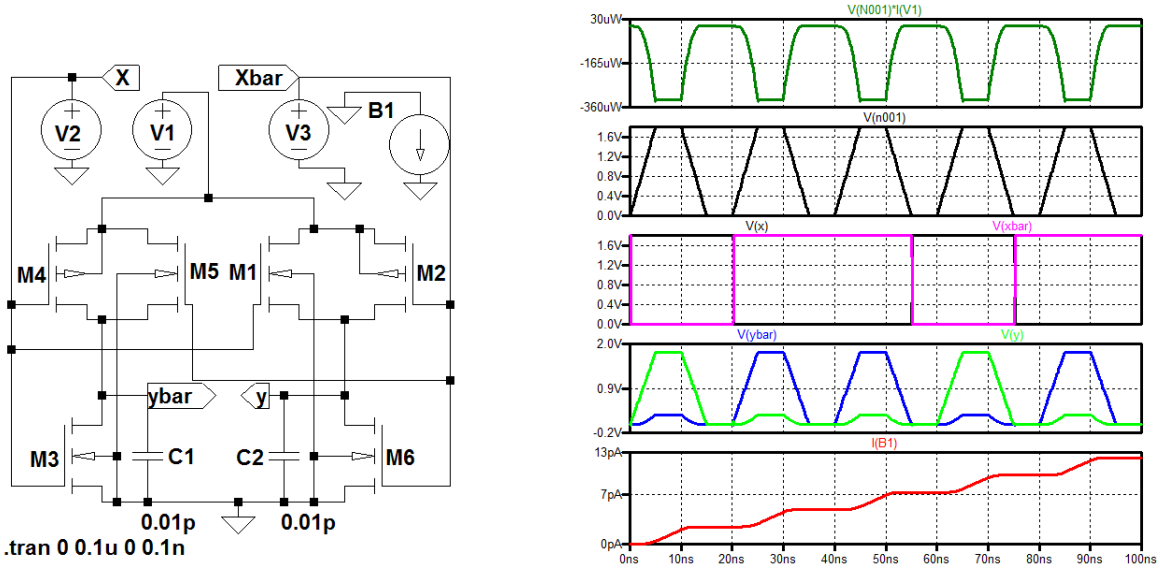

Fig. 1 2n2p-2n adiabatic logic circuits diagram and waveforms

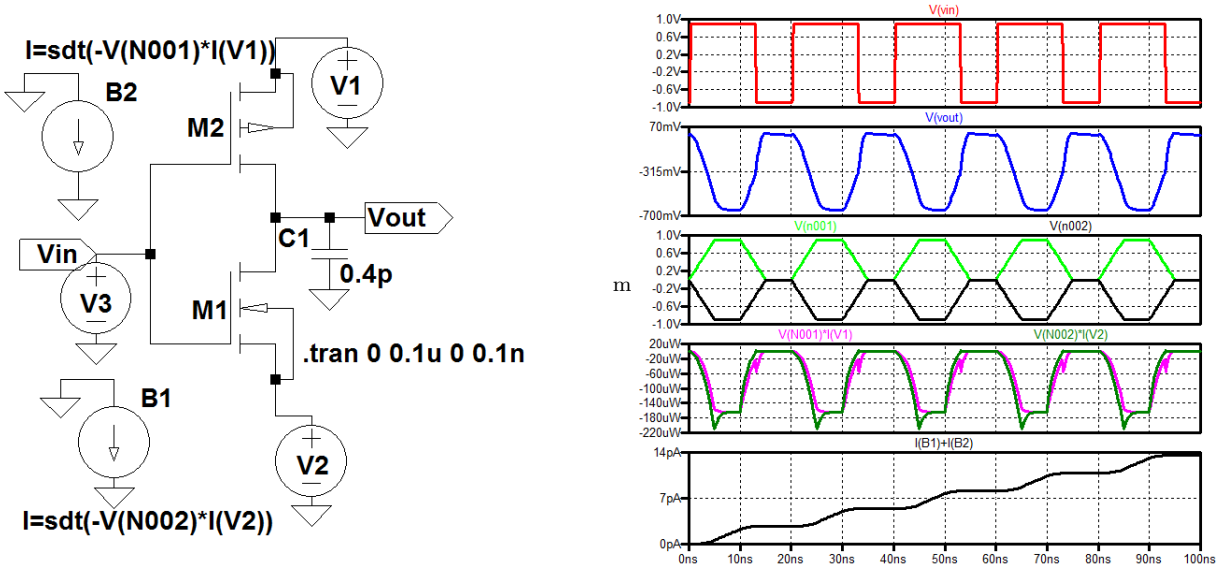

Fig. 2 Split level pulse 1n1p logic: circuits diagram and waveforms

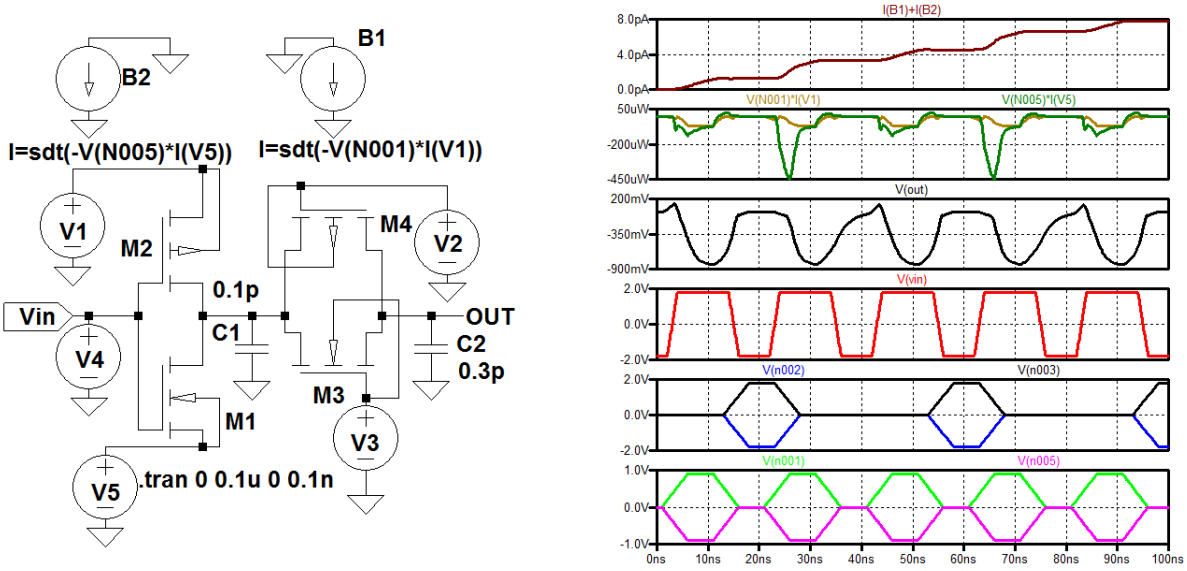

Fig. 3 Split level charge-recovery logic circuits diagram and waveforms

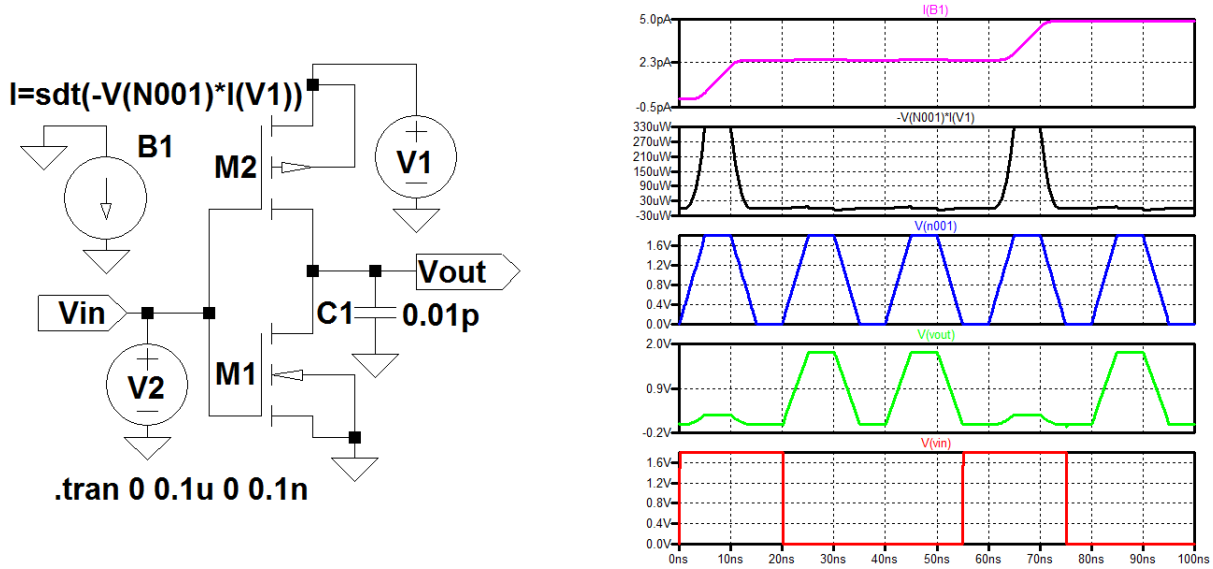

Fig. 4 1n-1p quasi-adiabatic logic circuits diagram and waveforms

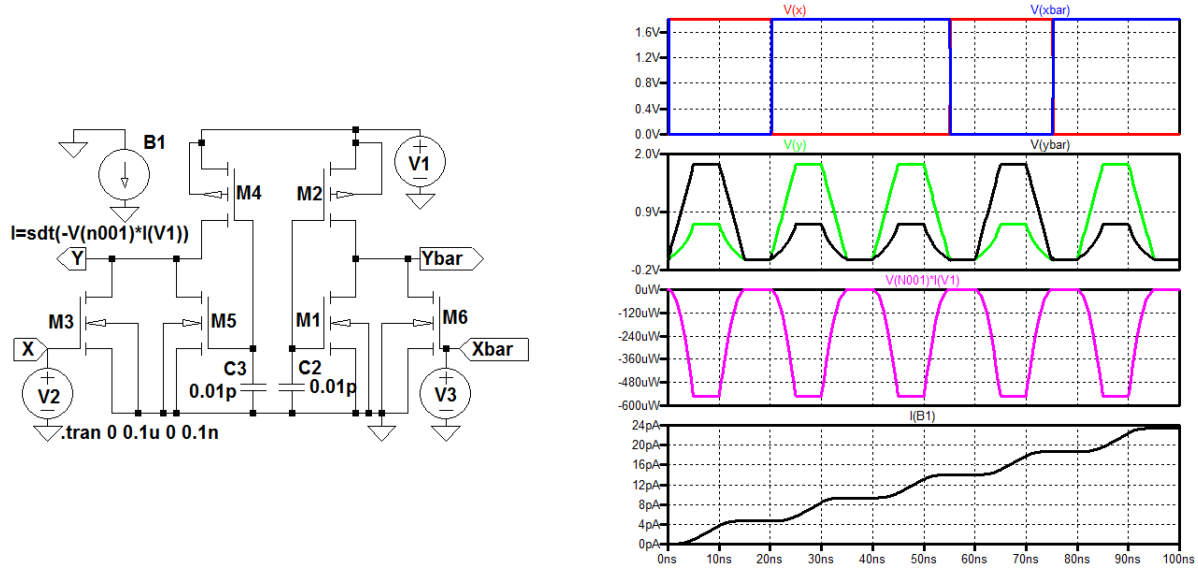

Fig. 5 2n-2n2p quasi-adiabatic logic circuits diagram and waveforms

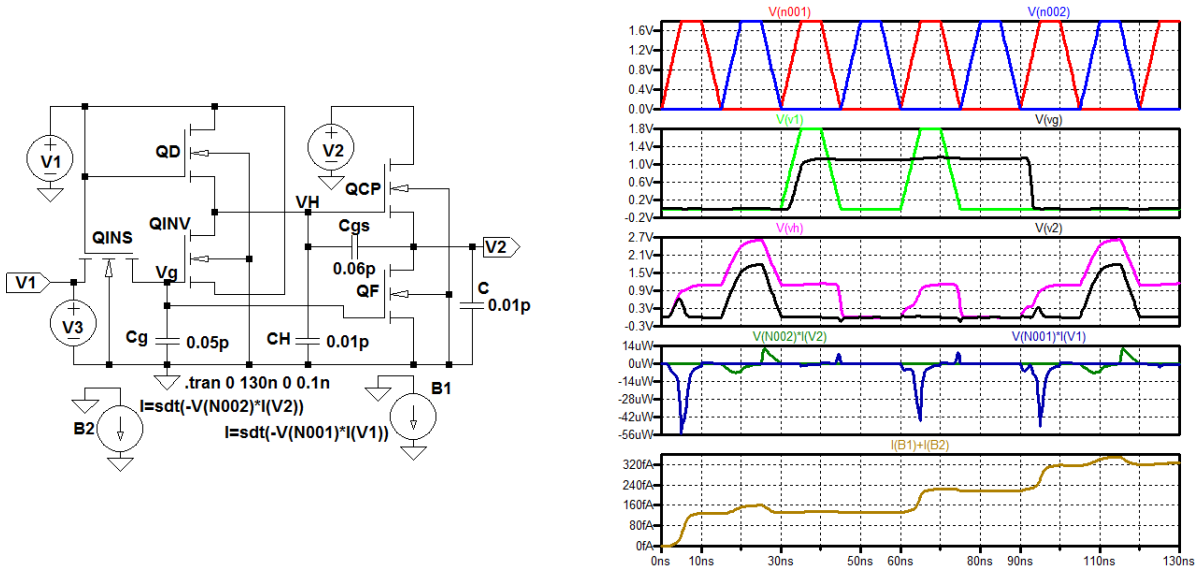

Fig. 6 Hot-clock nMOS logic circuits diagram and waveforms

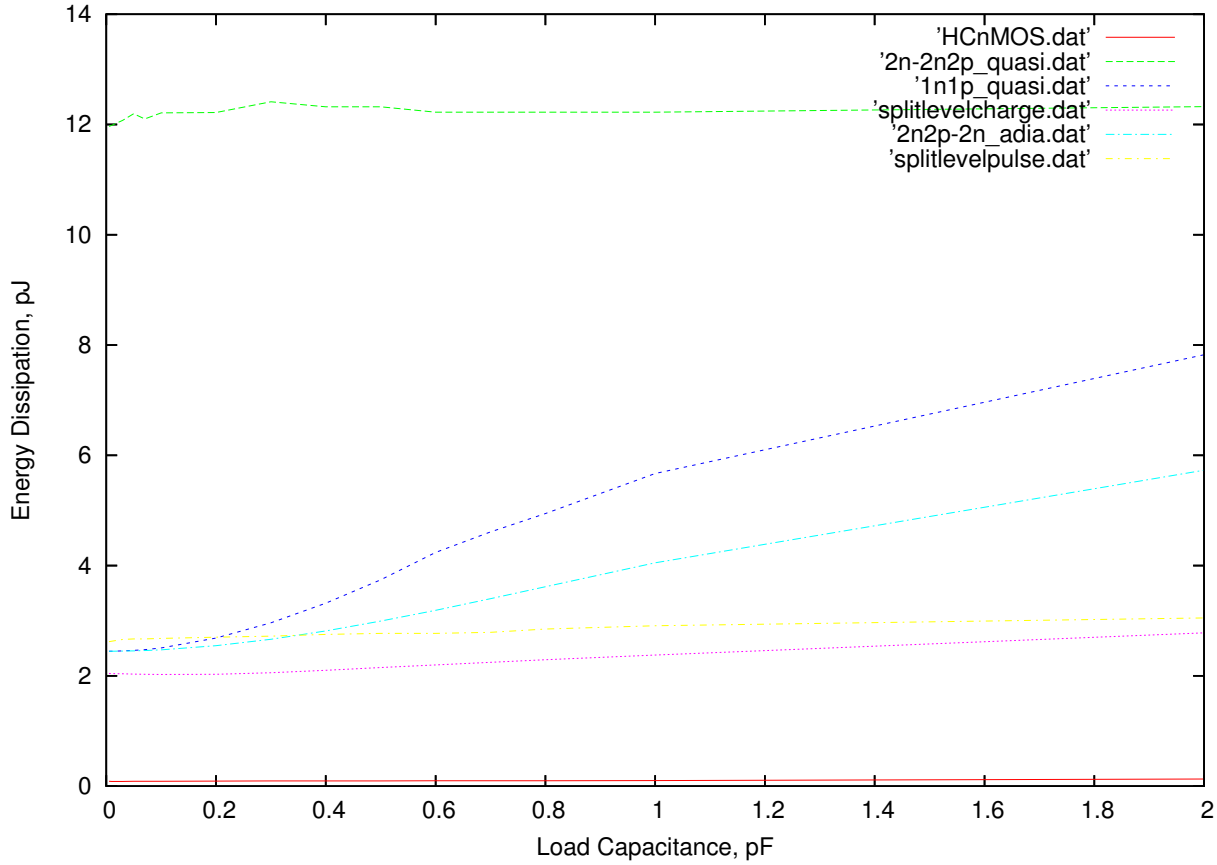

Fig. 7 2n2p-2n adiabatic logic circuits and waveforms