

Two Phase Clocked Adiabatic Static Logic Circuit: A Proposal for Digital Low Power Applications

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Abstract

This paper proposes a new quasi adiabatic logic family that uses two complementary pulsed supply clock for digital low power applications such as sensors. The proposed two-phase adiabatic static CMOS logic circuit (2PASCL) has switching activity that is lower than dynamic logic and can be directly derived from static CMOS circuits. We have done a SPICE simulation on the chain of four 2PASCL inverters implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the gates. The results show that 2PASCL can save a maximum of 63.3% of power dissipation over static CMOS logic at transition frequencies of 50MHz to 100MHz.

Conventional CMOS vs. 2PASCL

When a conventional CMOS which consists of the pull-up and pull down networks connected to a load capacitance C_L is set into a logical '1' state, an energy of $E_{applied} = C_L V_{DD}^2$ is applied to the load [1]. Energy stored is half of the energy supplied, therefore the total dissipation as heat during charging and discharging is the same as $E_{total} = C_L V_{DD}^2$. Whereas energy dissipation in the channel resistance R is given as $E_{diss} = \left(\frac{RC_L}{\Delta T}\right) C_L V_{dd}^2$. For adiabatic charging, when ΔT , which means the time for the driving voltage to change from 0V to V_{dd} is long, in theory, the energy dissipation is nearly zero.

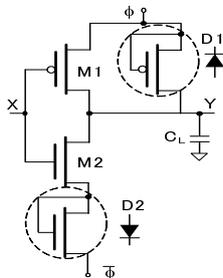


Fig. 1 2PASCL inverter circuit.

Figure 1 shows an inverter circuit of 2PASCL. The configuration of diodes using pMOS and nMOS are used to recycle the charge from the output. When the input, X is Hi, as ϕ swing up and $\bar{\phi}$ swing down, discharging via nMOS and D2 resulting the output logical state as '0' which is also known as 'evaluate' mode [2]. Next, as ϕ swing down and $\bar{\phi}$ swing up, it remains '0' where the circuit is in 'hold' mode. When the input is Low, and ϕ is swing up the circuit is in the 'charging' mode where C_L is charged through pMOS transistor. Discharging through D1 starts when ϕ swing down. The 'hold' mode reduces the transition activity which decrease the energy dissipation.

Simulation and results

The simulation of chain 2PASCL inverter circuit as in schematic diagram of Fig. 2 has been done. Its func-

tion is evaluated using the output waveforms graph. At input frequency of 1 to 100MHz, a power dissipation per cycle comparison to static CMOS chain inverter is as demonstrated in Fig. 3. Lower clock voltage frequency gives a lower power dissipation, P . P increases with the increasing transition frequency, f . From 10 to 100MHz, 2PASCL at 125Mhz clocking voltage shows a lower result compared to CMOS logic.

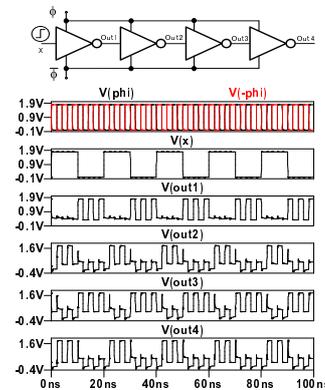


Fig. 2 2PASCL chain inverter circuit and simulation results.

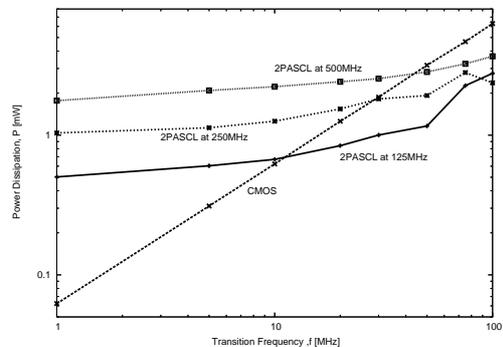


Fig. 3 Power dissipation at different transition frequency.

Conclusion

In this paper a two-phase adiabatic static logic (2PASCL) circuit has been proposed. The functional in four chain inverters has been confirmed and the power dissipation per cycle is 63.3% lower than conventional static CMOS logic.

References

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- [2] Y. Takahashi, Y. Fukuta, T. Sekine, and M. Yokoyama, "2PADCL: Two phase drive adiabatic dynamic CMOS logic," in Proc. IEEE Asia-Pacific Conf. Circuits Syst., pp. 1486-1489, Dec. 2006.