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低電力断熱的論理回路のシミュレーションと消費エネルギーの比較

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あらまし　この論文は入力遷移に関連しているエネルギー消費に関して低パワーの断熱論理ゲートの設計手法を調査します.SPICE を使用するコンピュータ・シミュレーションが 0.18μm CMOS 技術を使用することで実行されたいくつかのインバータ回路に行われます. V_{dd} と等しい高さに従った駆動するパルスを論理ゲートに供給します. また、消費の特性は異なった負荷キャパシタンス値で比較されます.
キーワード　低電力, 断熱論理

Low-power Adiabatic Logic Circuit: Simulation and Energy Dissipation Comparison

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Abstract　This paper investigates the design approaches of low-power adiabatic logic gates in terms of energy dissipation associated with the input transition. A computer simulation using SPICE is carried out on several inverter circuits implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the logic gates. The dissipation characteristics are also compared at the different load capacitance values.
Key words　low power, adiabatic logic

1. Introduction

The development of CMOS technology provides high density and high performance to integrated circuits. As the density of an integrated circuit increases, the power consumption increases and its temperature control becomes difficult. Moreover, mobile devices require a high performance, light weight, and long operation time, which are contradictory characteristics. Adiabatic circuits which are able to dissipate less energy than the fundamental limit of static CMOS are promising candidates for low-power circuits in the frequency range in which signals are digitally processed. In recent years, studies on adiabatic computing have been grown for low-power systems and several adiabatic logic families have been proposed.

In this paper we examine the functional and energy dissipation of adiabatics circuits using computer simulation. We also present a comparative study of the adiabatic circuits found in the literature with the conventional static CMOS designs. We also simulate the effects of the load capacitance to the energy dissipation.We conclude with a discussion of directions for further research in adiabatic design.

1.1 Adiabatic Logic Circuit Group

The adiabatic circuits are classified into asymtotically adiabatic and quasi-adiabatic circuit [1] based on whether full energy recovery or partial energy recovery is obtained.

1.1.1 Asymptotically Adiabatic Logic

Asymptotically adiabatic logic comprised of circuits in which dissipation results solely from finite rate of change of driving voltage and can be decreased to any desired level. It is represented by 2n2p-2n logic [2] [3], 1n1p logic that is using the split-level driving pulses [4] and split-level charge-recovery logic [5].

1. 1. 2 Quasi-Adiabatic Logic

Quasi-adiabatic logic [1] is comprised of circuits which dissipation can be reduced appreciably by lowering the rate of change of driving voltage. It is divided into another 2 groups, which is the static approach and the dynamic approach. The static is represented by 1n-1p [6] and 2n-2n2p quasi-adiabatic logic [7], Adiabatic Dynamic Logic (ADL) [8] [9], Efficient charge-recovery logic (ECRL) [10], Adiabatic Dynamic CMOS Logic (ADCL) [11], 2-Phase Adiabatic Dynamic CMOS Logic (2PADCL) [12] and 2n-2n2d [13]. The dynamic approach is represented by Hot-Clock nMOS (HCnMOS) logic [14], Recovered-Energy logic (REL) [15] [16].

2. Simulation and Results

2. 1 Conditions

The paper starts by examining the functional and energy dissipation of a simple logic gate, an inverter. The following test methodology was utilized. The simulations using LTSpice are carried out for all the inverters in this paper. The W/L of nMOS and pMOS logic gates used is 0.18 μm 0.6 μm. The output loads are driven by a clocking waveform ϕ which moves energy into and out of each gate. Circuits are connected to the input signal according to the layouts. A capacitive load of 0.01 pF is placed at each output node. Using trapezoidal power clock with 1.8 V peak-to-peak voltage, the output waveform at 50MHz frequency is shown in Fig. **??** – Fig. **??**, where the input signals are CMOS-compatible rectangular pulses, while the output signals are clocked signals. The top graph shows the input data. The second graph shows the pulse driving voltageoutput waveform. The third graph shows the output waveforms of a correctly functioning inverter. The bottom graph shows the energy dissipation of the logic gates which was simulated with the LTSpice software. It can also be calculated by integrating the voltage and current product value as follows

$$E = \int_0^{T_s} \left(\sum_{i=1}^{n} (V_{pi} \times I_{pi}) \right) dt \qquad (1)$$

where T_s is the period of the primary input signal, V_p is the power supply voltage, I_p is the power supply current and i is a number of power supply [2].

2. 2 Circuits comparison

Table 2. 2 lists the features of all logics in the review for comparison. In this preliminary results, ADL show the lowest value of energy dissipated per cycle while 2n-2n2p quasi adiabatic show the highest. 7 out of 10 adiatic circuits show a lower energy dissipation compared to conventional static CMOS by reducing from 98% to 17%.

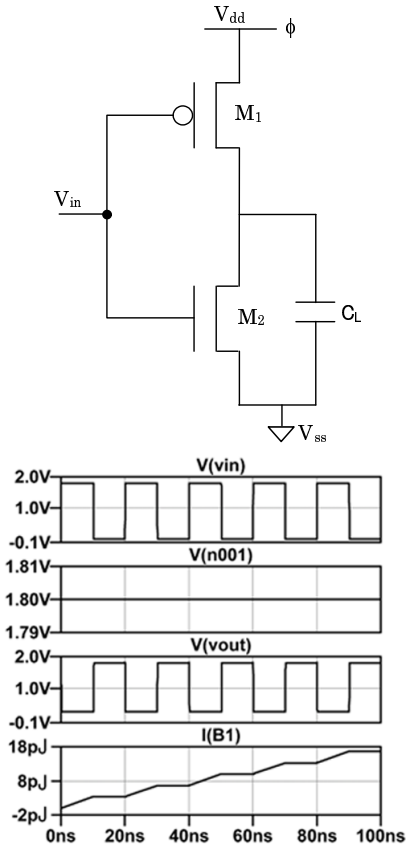

Fig. 0 Conventional CMOS logic inverter circuit diagram and waveforms

Table 0 Comparison of Power Dissipation

Adiabatic Logic	Energy(pJ/cycle)	Gates	Driving Pulse
ADL	0.035	4	4
2n-2n2D	0.116	6	1
ADCL	0.133	4	1
HCnMOS	0.60	5	2
1n-1p SLCR	0.68	4	1
2PADCL	0.77	4	2
1n-1p SLP	0.86	2	2
1n-1p quasi	2.04	2	1
CMOS	3.33	2	1
2n2p-2n	3.45	6	1
ECRL	3.61	4	1
2n-2n2p quasi	5.69	6	1
REL (MOSFET)	9.24	4	1

2. 3 Energy dissipation at different load capacitance

The simulation result on the energy dissipation at different load capacitance is shown in Fig. 2. 3. As expected, all the circuits, except 2PADCL show an increase of dissipated energy when changing the load capacitor to a higher value.

3. Discussion

Analysis of the adiabatic circuits using LTSpice shown that

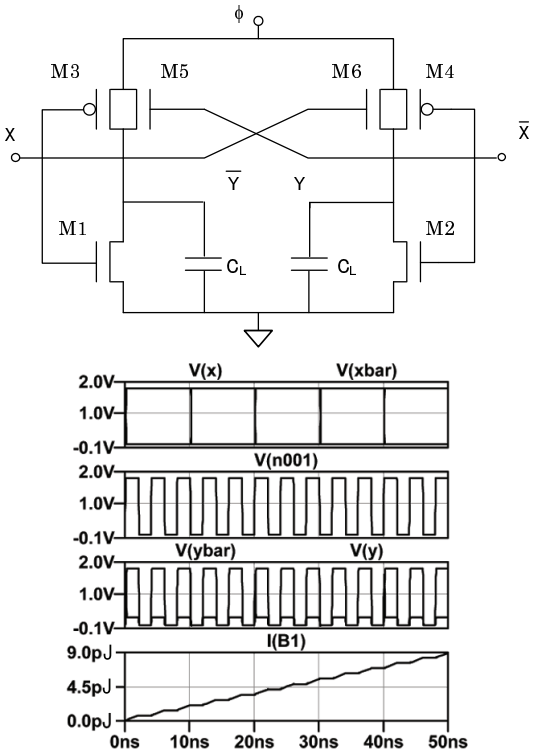

Fig. 0 2n2p-2n adiabatic logic inverter circuit diagram and waveforms

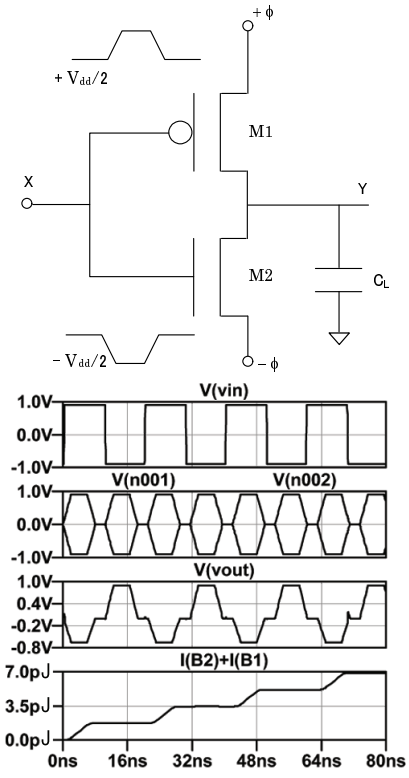

Fig. 0 Split level pulse 1n1p logic inverter circuit diagram and waveforms

the energy dissipation per cycle can be calculated and therefore is convenience for futher analysis and design. In this simulation result, ADL shows the lowest energy dissipation as an inverter. Load Capacitance which use as the data holder

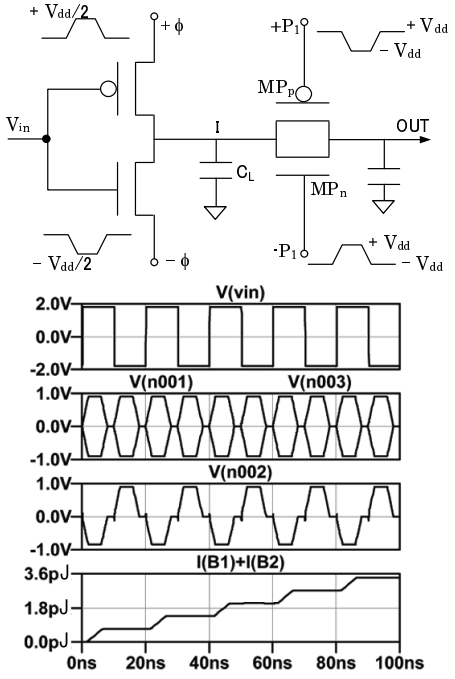

Fig. 0 Split level charge-recovery logic inverter circuit diagram and waveforms

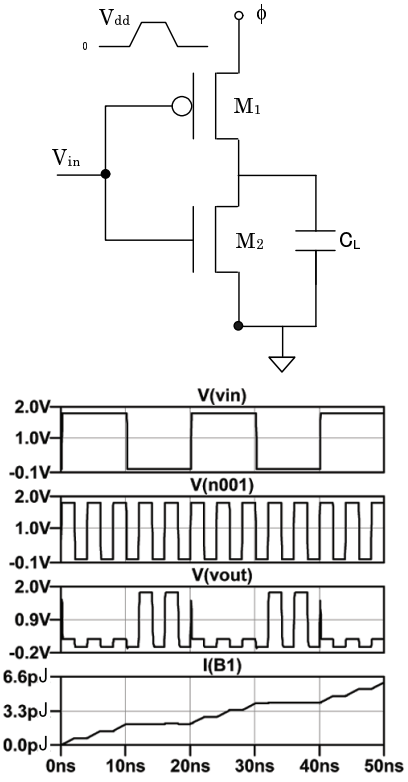

Fig. 0 1n-1p quasi-adiabatic logic inverter circuit diagram and waveforms

need to be design precisely considering the time constant that effect the output and also the amount of information to be stored. Unlike other circuits 2PADCL shows a decrease in energy dissipation when the load capacitance increased. If this is true, this circuit has a higher possibility to be further studied. REL in MOSFETs circuits are still not operating

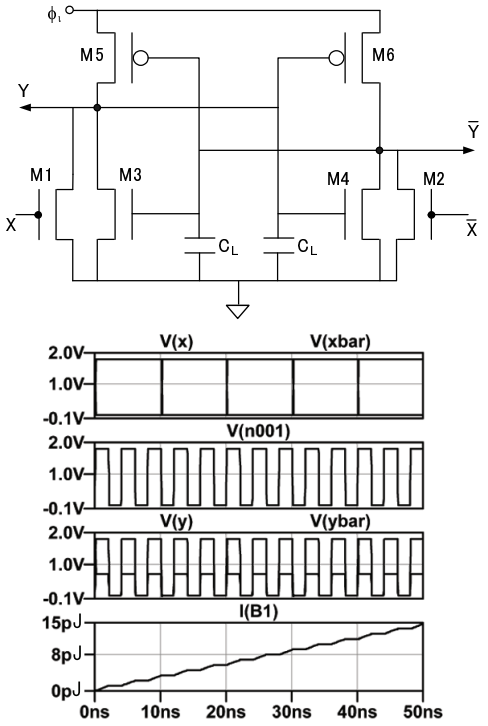

Fig. 0 2n-2n2p quasi-adiabatic logic inverter circuit diagram and waveforms

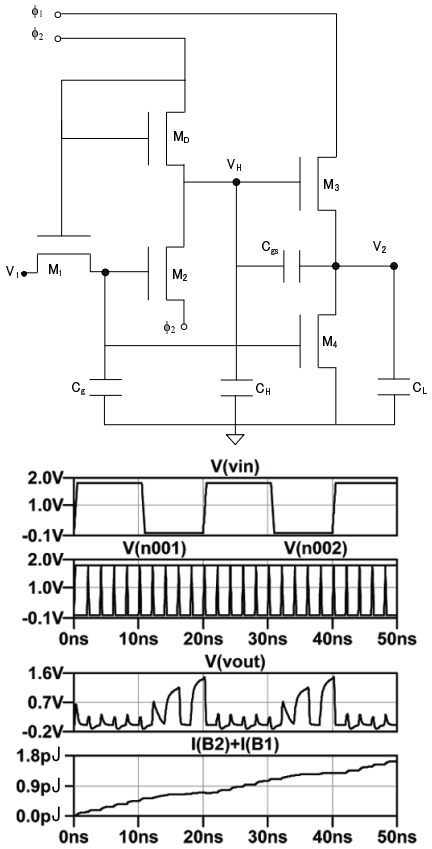

Fig. 0 Hot-clock nMOS logic inverter circuit diagram and waveforms

very well in this simulation.

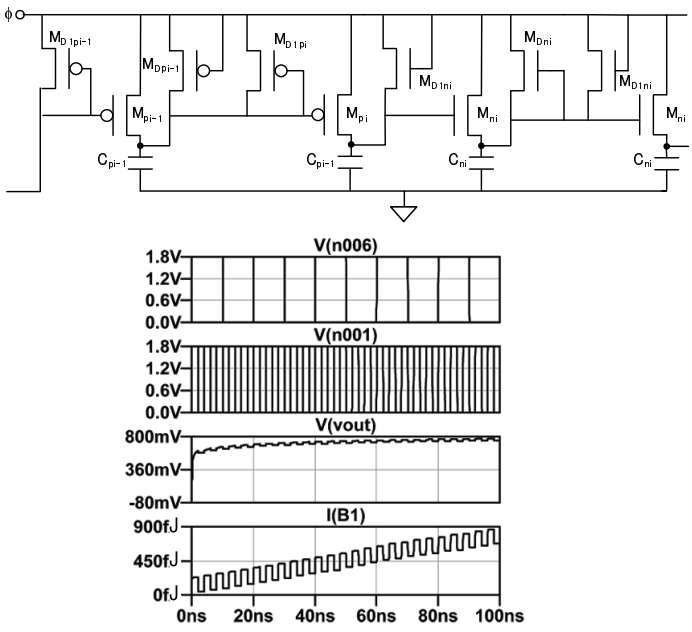

Fig. 0 Recovered-energy logic (REL) in MOSFETs inverter circuit diagram and waveforms

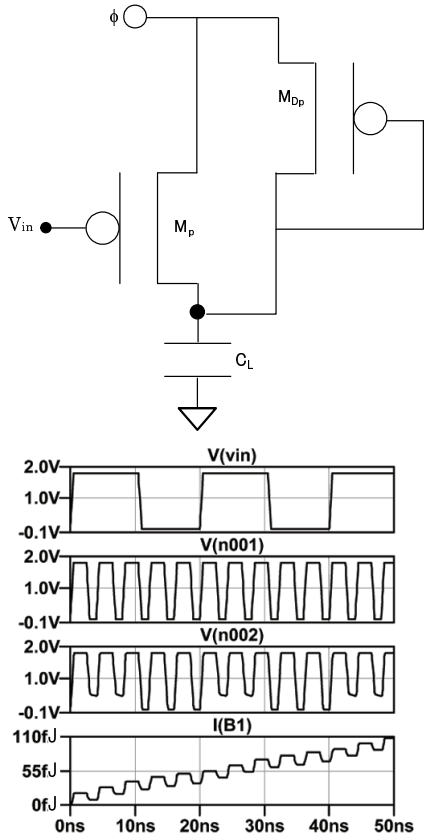

Fig. 0 Adiabatic Dynamic logic (ADL) inverter circuit diagram and waveforms

4. Conclusion

We have done simulations to find out the functional and energy dissipation characteristic of each adiabatic logic circuits. The LTSprice simulations using trapezoidal power clock prove that the designed circuits have the correct logic

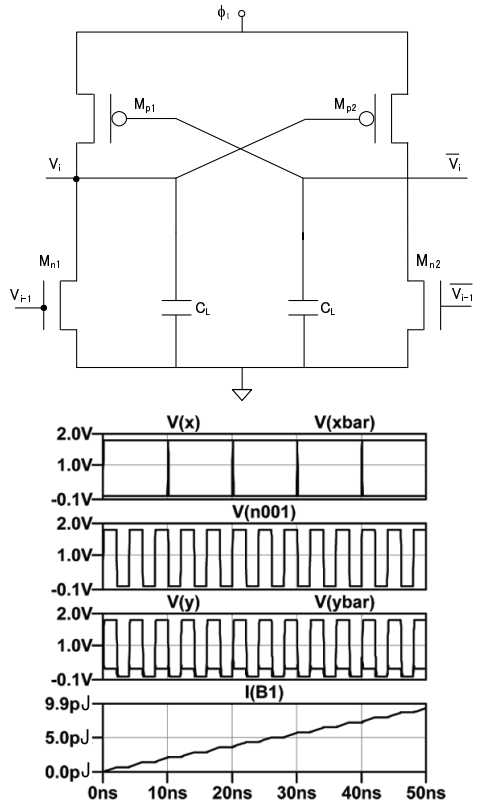

Fig. 0 Efficient charge-recovery logic (ECRL) circuit diagram and waveforms

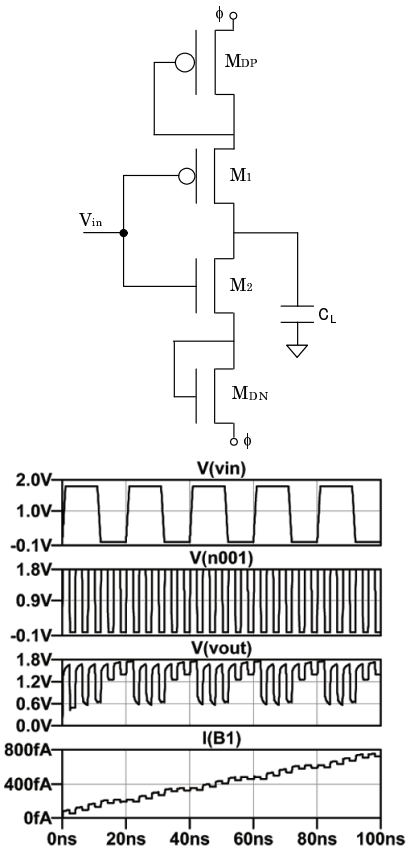

Fig. 0 Modified Adiabatic Dynamic CMOS logic (ADCL) circuit diagram and waveforms

function and considerable energy saving. The design principle can also be used for designing more complicated adiabatic CMOS circuits. We conclude that most of the proposed circuits have lower energy dissipation compared to conventional CMOS logic.

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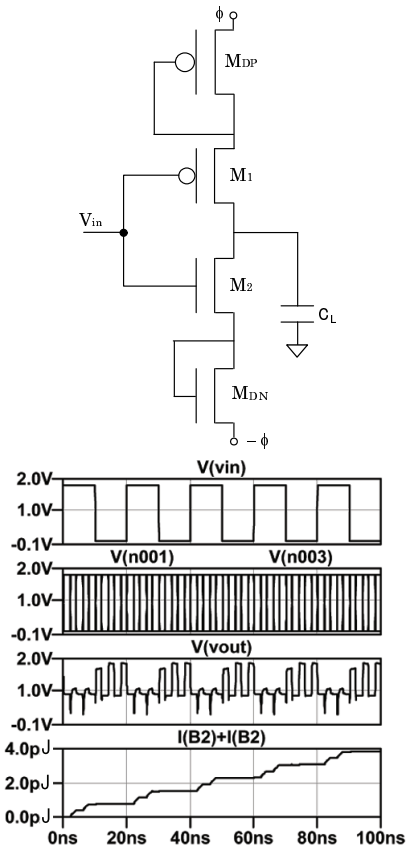

Fig. 0 Two-phase drive adiabatic dynamic CMOS logic (2PADCL) circuit diagram and waveforms

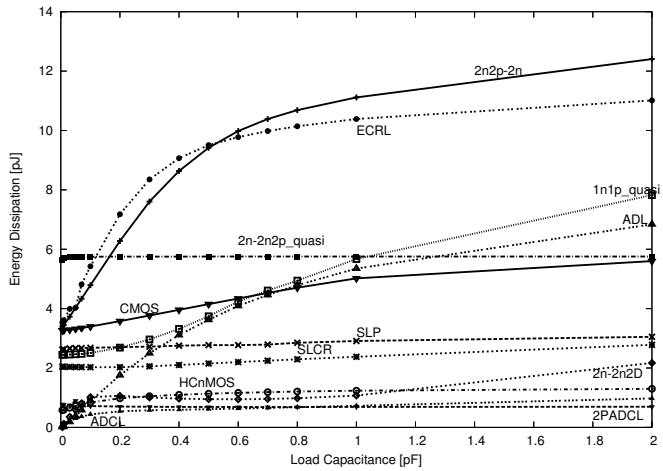

Fig. 0 Energy dissipation comparison in adiabatic circuits at different load capacitance value

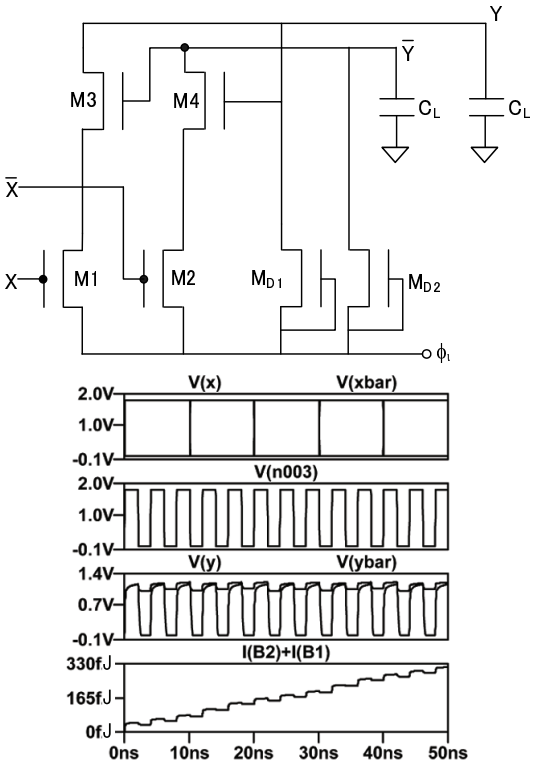

Fig. 0 2n-2n2D circuit diagram and waveforms