# Thermal Characterization and Electrical Performance of Low Profile Power Packages

Nazrul Anuar, Ng Cheong Chiang
ChipPAC Malaysia Sdn. Bhd.
73, Lorong Enggang, Ulu Kelang FTZ, 54200 Kuala Lumpur, Malaysia
Nazrul.Anuar@ChipPAC.com, CC.NG@ChipPAC.com

**Abstract**

Increasing demand for low profile and low cost power packages for use in commercial applications drives the development of these packages with competitive cost advantage. The objective of this study is to compare the thermal and electrical performance of thinner version power packages. Both modeling and experimental works are resorted to analyze package robustness. While a large package will guarantee a lower thermal resistance, many applications are very restrictive in terms of the space available for the devices – it is in such applications that a small discrete device has advantages over the module [1].

## 1. Introduction

When designing a high current plastic package, there are many factors to be considered. As the current increases to the device limits, the die temperature and the package temperature would be at their respective limits. The $R_{DS(ON)}$ of a power MOSFET increases with the temperature. With the resistance increases, the power dissipated for a constant on-current increases, the junction temperature, Tj increases and resistance further increases until the devices is in thermal equilibrium with the heat removal system [2].

There are other factors that contribute $R_{DS(ON)}$ in a package other than the on-resistance of the die itself. They are the resistance of the wire used for the bonding, resistance of the solder used for die attaches and the $R_{DS(ON)}$ varies as material used for the leadframe frame varies. The lower heat dissipation of the header where the dies are attached can also contribute to the higher $R_{DS(ON)}$ value.

For this evaluation, the packages studied are DPAK (package thickness: 2.3 mm), D2PAK (package thickness: 4.4 mm) and T2PAK (package thickness: 2.2 mm). The leadframes under evaluation are Single Gauge DPAK (test) to Dual Gauge DPAK (control), and T2PAK (test) to D2PAK (control). These thinner leadframes will give a significant material cost reduction. For the Single Gauge (SG) DPAK, the difference is at the header, where it is 15 mil thinner than the header of the Dual Gauge (DG) DPAK. For T2PAK, the header is 40 mil thinner than the header of the D2PAK. Both low profile packages have compatible foot print with relative existing packages.

The electrical performance of these low profile power packages is compared using $R_{DS(ON)}$ and Delta $V_{SD}$ tests. Most power dissipated by a MOSFET is due to the $R_{DS(ON)}$ value. The Delta $V_{SD}$ test is normally used to screen for poor die attach where huge solder voids are present either between the solder and die back or between solder and leadframe pad.

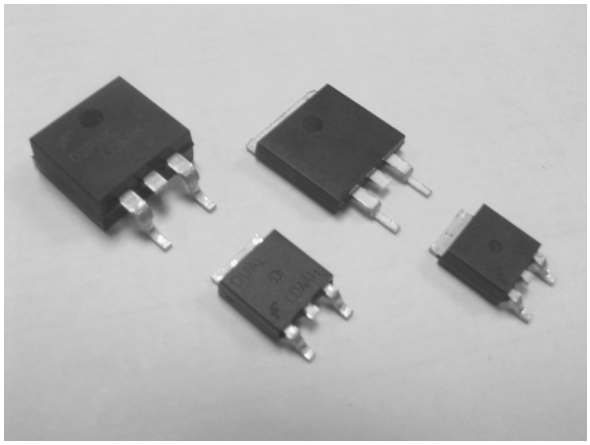

**Fig. 1 D2PAK, T2PAK, SG and DG DPAK**

Such solder void reduces the effective area of contact between the die back and the leadframe thus it will avoid the good transfer of heat from the silicon junction of the device to the heatsink.

This effect of a poor heat transfer will be a higher Tj for the device and affects the overall performance of device under test. The percentage difference of $R_{DS(ON)}$ and Delta $V_{SD}$ on the said different leadframe thickness and material is determined while maintaining the other factors, i.e. wire diameters, die, solder and mold compound as constant.

The heat dissipation is poorer in the T2PAK leadframe as the die bond pad volume is about 65% smaller than the D2PAK. For thinner and low volume leadframe, residual heat may increase the resistance between the inner part of the header to the heatsink. However, for some consumer applications, certain requirement criteria can be reduced to meet certain market segment price expectation.

For this experiment, about 200 units for each package has been assembled with Trench technology MOSFET dies, 100W x 132L x 8T mil. Wire configuration for this device is 2 X 12 mil for Source wire and 1 X 8 mil for Gate wire. Header or die attach pad thickness for D2PAK is 50 mil, T2PAK is 10 mil, SG DPAK is 20 mil and DG DPAK is 35 mil. Thermal conductivity for different leadframe material is shown in Table I.

All units are then electrically tested using Kelvin type manual socket. For the $R_{DS(ON)}$, devices is supplied with two different $V_{GS}$, 4.5V and 10V while $I_D$ is biased at 50A. For the Delta $V_{SD,}$ parameters set as $V_{SD}$=10V, $I_D$=1.5A, Pt=100ms, Dt=40us, GLM = 20V. Testing is done in a 24°C/50%RH controlled environment.

## 2. Thermal Characterization

Both modeling and experimental works were resorted to analyze the package robustness. Finite element model of the packages was generated to compare the package heat dissipation capability by looking at the temperature distribution of the model. In order to exclude the package geometry effect, the thermal performance of the package was further studied using the same package with different device powers and package materials of different thermal conductivity.

Both low profile packages have compatible footprint with relative existing packages, as shown in Fig. 2. These packages have been assembled using four different leadframe materials, as recorded in Table 1. They have different thermal conductivity and electrical resistivity.

**Fig. 2 Compatible footprint of low profile package**

In this study, three-dimensional solid model was generated to determine the temperature distribution of the package. Due to symmetry of the package so as the deformation, only half of the package was simulated with symmetrical boundary condition imposed. As shown in Fig. 3, the FEA model has silicon die, die attach, leadframe, molding compound, and PCB test board, which consists of PCB mask, copper conductor traces and PCB core. The temperature dependency of the material properties was considered in the calculations.

**Table I Thermal conductivity of different leadframe material**

| Package | SG DPAK | DG DPAK | T2PAK | D2PAK |
|---|---|---|---|---|
| Thermal Cond. (W/mK) | 351 | 364 | 263 | 347 |

Temperature dependent flat plate correlations, which account for both radiation and convection heat transfer, were employed to calculate surface boundary conditions for natural convection environments i.e. still air. The reader is referred to the technical publication [3] for the correct application of these surface convection and radiation boundary conditions. Using reference [3], the free convection coefficients for a JEDEC standard test environment [4] were calculated using the dual surface isoflux flat plate correlation equations. Device power of 1.0W was applied with ambient air temperature of 24°C.

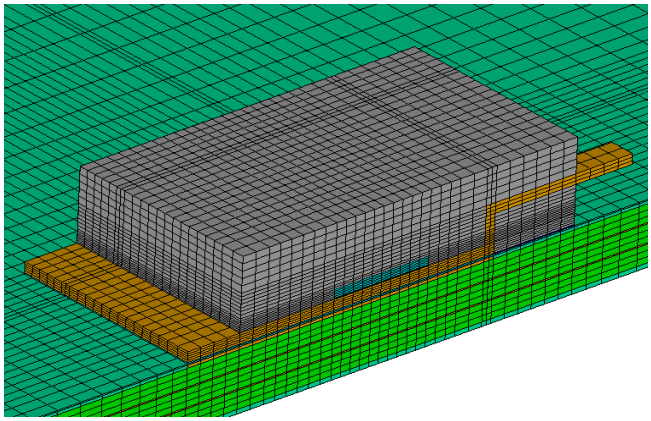

**Fig. 3 Finite element model**

For the first FEA study, the models were built using the same material set as the electrical test. As shown in Fig. 4, D2PAK has the lowest die temperature. T2PAK was about 15% higher temperature than D2PAK. However, SG DPAK was less than 1% higher temperature than DG DPAK. The die temperature increased with decreased leadframe thickness because of the thermal “capacitance” of the package was reduced. Confirmation run was performed by using a same set of material for all the four packages. The highest die temperature for the respective package did not vary significantly. Hence, the package volume has a larger effect on the package heat dissipation capacity compared to the package materials.

The effect of leadframe material on the package heat dissipation was investigated in the second FEA study. Four different thermal conductivity of the leadframe was chosen by using T2PAK and D2PAK. Fig. 5 shows the temperature distribution of T2PAK by using leadframe thermal conductivity of 350W/mK. The relation between leadframe thermal conductivity and die highest temperature generated was plotted in Fig. 6. When the leadframe thermal conductivity increased three times from 150W/mK to 450W/mK, the die temperature only decreased 2.0% for T2PAK and 1.4% for D2PAK. Thus, the leadframe material did not provide a significant contribution to the package heat dissipation.

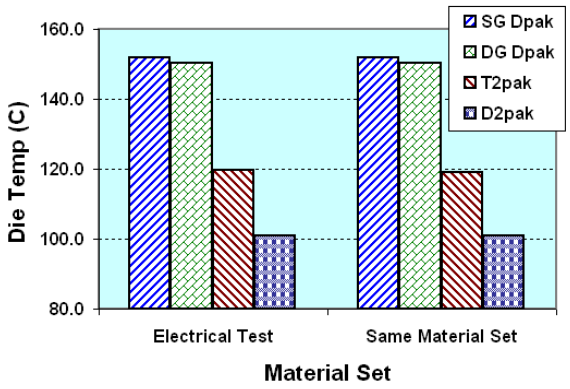


**Fig. 4 Highest die temperature**

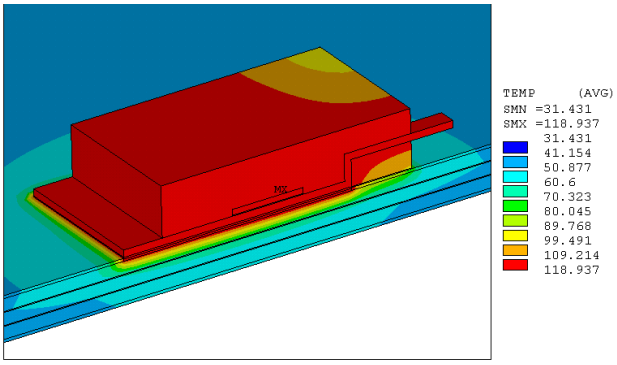


**Fig. 5 Temperature distribution of T2PAK**

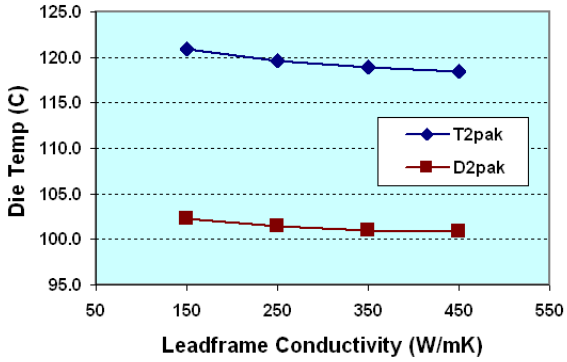


**Fig. 6 Highest temperature for T2PAK and D2PAK**

In the third FEA study, the effect of die attach material on the package heat dissipation was investigated. T2PAK and D2PAK were used with four different thermal conductivity of the die attach material. Temperature distribution of D2PAK by using die attach material of thermal conductivity 40W/mK are shown in Fig. 7. The molding compound elements are excluded for a better visualization. Fig. 8 compared the relation between die attach material thermal conductivity and die highest temperature generated. The die temperature only decreased 2.9% for T2PAK and 2.5% for D2PAK when the die attach material thermal conductivity increased twelve times from 5.0W/mK to 60W/mK. Therefore, the die attach material also did not contribute much to enhance the package heat dissipation.

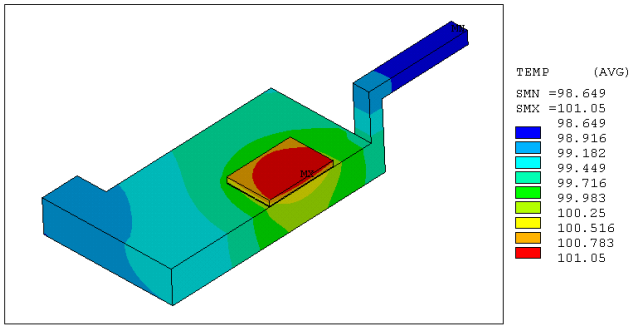


**Fig. 7 Temperature distribution of D2PAK**

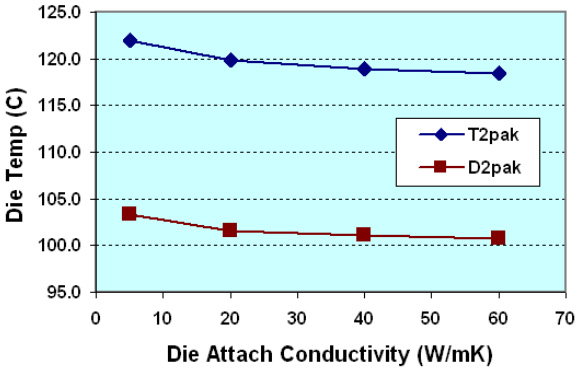


**Fig. 8 Highest temperature for T2PAK and D2PAK**

The effect of device power on the package temperature was investigated in the last FEA study. Four different device power was chosen by using SG DPAK and DG DPAK. Fig. 9 shows the temperature distribution of SG DPAK by using device power of 1.5W. The relation between device power and die highest temperature generated was plotted in Fig. 10. When the device power increased four times from 0.5W to 2.0W, the die temperature increased three times for SG DPAK and DG DPAK. Thus, the device power has a very strong effect on the package temperature.

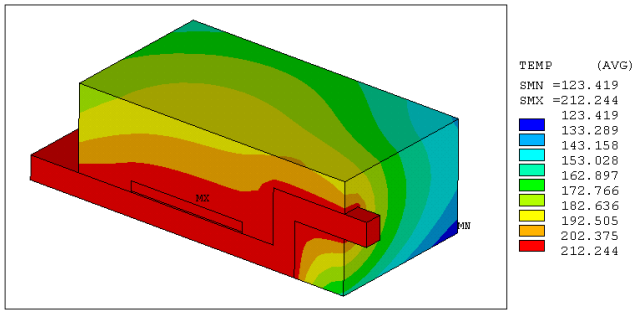


**Fig. 9 Temperature distribution of SG DPAK**

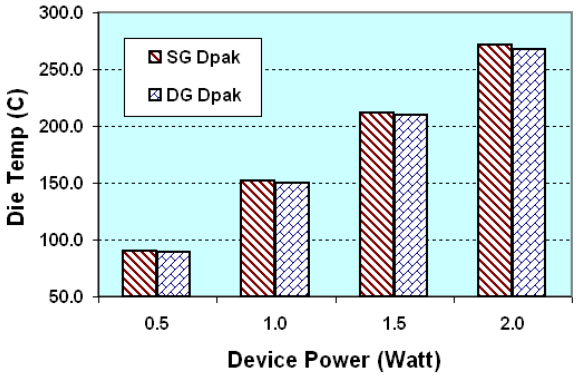


**Fig. 10 Highest temperature for SG DPAK & DG DPAK**

## 3. Electrical Performance

The results are as shown in Fig. 11 to Fig.13.

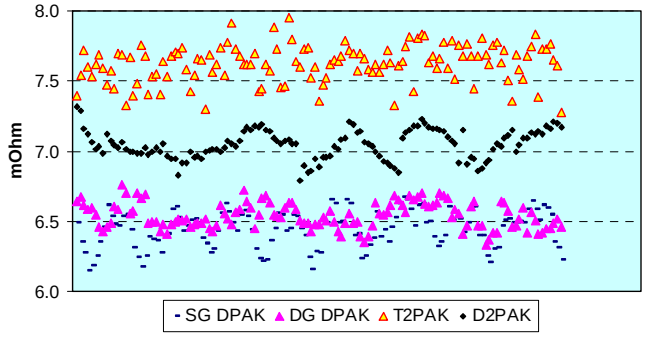


**Fig. 11 $R_{DS\ (ON)}$ 1, $V_{GS}$= 4.5V**

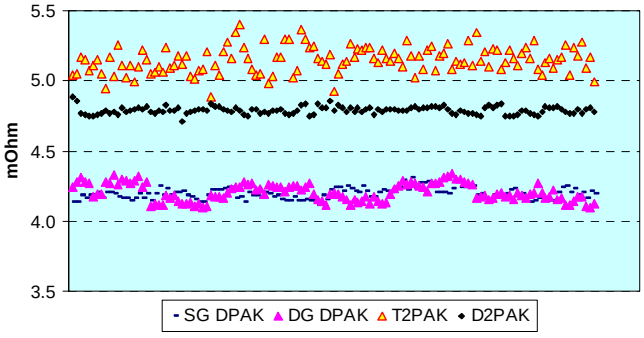


**Fig. 12 $R_{DS\ (ON)}$ 2, $V_{GS}$= 10V**

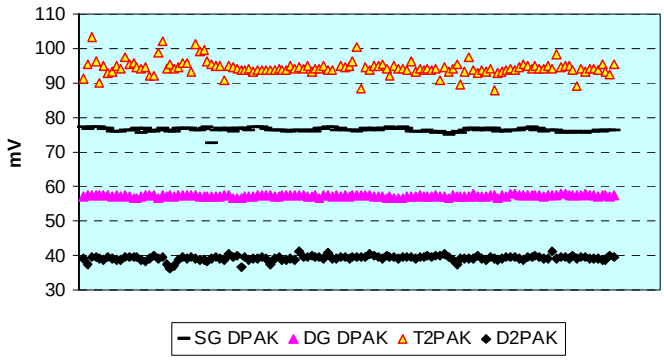


**Fig. 13 Delta $V_{SD}$**

From the experiment, $R_{DS(ON)}$1 for SG DPAK is 1.48% lower than DG DPAK. The $R_{DS(ON)}$2 for SG DPAK is 0.23% lower than DG DPAK. For $R_{DS(ON)}$2 the readings are lower as we increased the $V_{GS}$ from 4.5V to 10V. This is because $R_{DS(ON)}$ is dependent on the Voltage biased to the Gate when referred to the Source. The higher the $V_{GS}$ value the lower the $R_{DS(ON)}$. $R_{DS(ON)}$1 for T2PAK is 8.17% higher than D2PAK. The results also show that $R_{DS(ON)}$ for T2PAK is 7.49% higher than D2PAK.

From the Delta $V_{SD}$ results, the average reading of SG DPAK is 33.24% higher compared to DG DPAK. T2PAK has 140.85% higher in Delta $V_{SD}$ compared to D2PAK.

**Table II Theoretical calculation of Electrical and Thermal Resistance**

| Package | SG DPAK | DG DPAK | D2PAK | T2PAK |
|---|---|---|---|---|
| Thermal Cond, W/m-K | 351 | 364 | 347 | 263 |
| Elect. Resist., Ohm-m | 1.90E-08 | 1.87E-08 | 1.92E-08 | 2.54E-08 |
| Thickness, | 5.08E-04 | 8.89E-04 | 1.27E-03 | 2.54E-04 |
| Area, m2 | 2.52E-05 | 2.52E-05 | 2.63E-05 | 4.56E-05 |
| R, Ohm | 3.83E-07 | 6.60E-07 | 9.27E-07 | 1.41E-07 |
| Rth, C/W | 5.74E-02 | 9.69E-02 | 1.39E-01 | 2.12E-02 |

For comparison between SG and DG, from above result and resistance table, we can conclude that; the difference in substrate electrical resistivity (diff: 1.6%), SG DPAK, that has 42% lesser DC Electrical Resistance and 41% lesser Thermal Resistance [5] gives only 1.43% lower $R_{DS(ON)}$. This shows that, leadframe material with has difference electrical and thermal conductivity has less effect on the package temperature.

For comparison between T2PAK and D2PAK, from above result, T2PAK which is 85% lesser in DC Electrical Resistance and 85% lesser in Thermal Resistance from junction to heatsink has 8.2% higher $R_{DS(ON)}$. This supports the fact that thicker leadframe with high profile packages give lower thermal resistance from junction to case.

We can conclude that heat dissipation is poorer in the T2PAK leadframe as the die attach pad volume measured for the T2PAK is 65% smaller than the D2PAK. This concludes that, for thinner and low package volume leadframe, residual heat increase the resistance between the inner part of the header to the heatsink.

For the Delta $V_{SD}$, we understand that since the die attach pad volume of SG is 10.5% smaller than SG, after power is supplied and cut off, heat dissipation is poorer compared to the DG DPAK. To ensure there is no solder die attach void for SG compared to DG, samples were inspected under X-ray for confirmation.

For the Delta $V_{SD}$ of T2PAK, we understand that since the die attach pad volume of T2PAK is 65% smaller than D2PAK, same as above phenomenon, after power is

supplied and cut off, heat dissipation is poorer compared to the D2PAK. Samples are also inspected for any solder die attach void. Based on the X-ray result (as shown in Fig. 14 and Fig. 15), it is found that no significant difference in the solder die attach void. Thus, the package volume has the biggest impact on the heat dissipation capability.

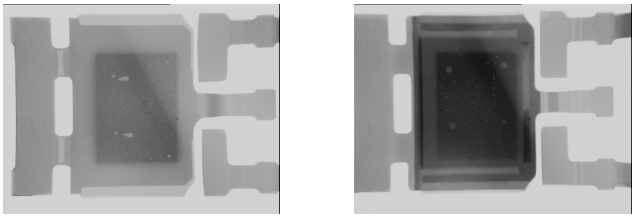

**Fig. 14 No significant die attach void for SG DPAK (left) compared to DG DPAK (right)**

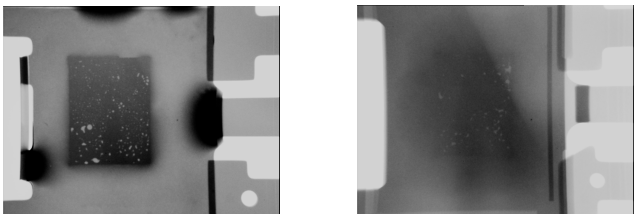

**Fig. 15 No significant die attach void for T2PAK (left) compared to D2PAK (right)**

## 4. Conclusions

From the FEA, it was found that the package volume has a larger effect on the package heat dissipation capacity compared to the package materials. When the leadframe thermal conductivity increased three times, the die temperature only decreased 2.0% for T2PAK and 1.4% for D2PAK. The die temperature only decreased 2.9% for T2PAK and 2.5% for D2PAK when the die attach material thermal conductivity increased twelve times from 5.0W/mK to 60W/mK. Hence, the leadframe and die attach materials did not provide a significant contribution to the package heat dissipation. When the device power increased four times from 0.5W to 2.0W, the die temperature increased three times for SG DPAK and DG DPAK. Thus, the device power has a very strong effect on the package temperature.

From the $R_{DS(ON)}$ performance, Single Gauge DPAK which has 10.5% smaller die attach pad volume but has the same package footprint and thickness resulted only 1.43% lower compared to Dual Gauge. For a larger difference, T2PAK which is 65% smaller die attach pad compared to D2PAK, the results show T2PAK has 8.2% higher reading. We can conclude that for $R_{DS(ON),}$ leadframe thickness is not really a factor but the bigger package volume, the better the heat dissipation resulted the lower $R_{DS(ON).}$

From the Delta $V_{SD}$ results, it shows that the heat dissipation performance increased from thinner to the thicker die attach pad according to SG DPAK and DG DPAK experiment. Significantly higher heat dissipation performance can be seen on the high profile package compared to low profile one based on T2PAK and D2PAK results.

The electrical properties are not considered in the thermal FEA studies. T2PAK leadframe which has the highest electrical resistivity gave the highest $R_{DS(ON)}$ and Delta $V_{SD}$ values in the electrical tests. Further experiments will be performed to study the effect of material electrical properties on the package temperature distribution.

As the conclusion from this overall result, the package volume has the largest effect on the package thermal and electrical performance. Thicker die attach pad gives a slightly better heat dissipation performance compared to the thinner die attach pad. Die attach material and leadframe material did not give significant difference in the thermal performance.

**Acknowledgments**

The authors would like to thank Bret Zahn, Saat Shukri and Eddie Lee for technical discussion

**References**

1. Pamela Dug dale, Arthur Woodworth, "Current Handling and Thermal Consideration in a High-Current Semiconductor Switch Package," *Darnell.Com Power Pulse*, (2001), pp. 4-5.
2. Jerrold Foutz, "Power MOSFET Thermal Runaway," *SMPS Technology Knowledge Base*, July. 2003, pp. 1-2.
3. Zahn, B.A., and Stout, R.P., "Evaluation of Isothermal and Isoflux Natural Convection Coefficient Correlations for Utilization in Electronic Package Level Thermal Analysis", *Proc 13th Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, January 1997.
4. EIA/JESD51-2: Integrated Circuit Thermal Test Method Environment Conditions – Natural Convection (Still Air).
5. Wharton McDaniel, "Thermal performance of MOSFET packages", *International IC –Taipei Conference*, pp. 102-103.