Power-Saving Analysis of Adiabatic Logic in Subthreshold Region

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***Abstract*—This paper reports a comparison of energy dissipation between different adiabatic logics in the subthreshold operation. In SPICE simulation we use a real industrial 0.18 μm BSIM3v3 model having a device parameter in the subthreshold region and then confirm the energy savings of quasi-adiabatic logic families, namely, 2N2N2P, 2PC2AL, CAL, ECRL, PAL, PECRL, PFAL, and SAL. From the results we show that the energy consumption of our previously proposed 2PC2AL inverter is lower than those of the other adiabatic logics, in the range of from 10 kHz to 10 MHz.**

Keywords*—adiabatic logic, subthreshold logic, low power, RFID, smart card*

I. Introduction

Power consumption has been becoming a limiting factor in integrated circuit technology as device sizes shrink. Applications such as wireless sensors, RFID tags have only a very small amount of power available to them, and therefore we should designed to use a minimum of energy. In the design of ultra low-power VLSI logic circuits with medium frequency of operation (300 kHz– 3 MHz), several novel techniques (e.g. adiabatic, subthreshold) have been proposed.

Adiabatic (or energy recovery) techniques [1]–[12] show great potential, because they are able to break the lower limit of the energy dissipation in static CMOS which amounts to $CV_{\rm dd}^2/2$. The different adiabatic logics that have been developed until now can be classified as Asymptotically adiabatic logics [1], [2], and Quasi-adiabatic logics [3]–[12]. The first category comprises structures that require computations to be reversible. The main idea behind the efficient operation of these architectures is to use the reverse computation for discharging in a controlled manner the capacitors that were charged during the forward computation. The second category is further classified into two groups: Rank-1 quasi-adiabatic [8], [9], and Rank-2 quasi-adiabatic [3]–[7], [10]–[12]. The rank-1 adiabatic circuits use diodes to circumvent the requirement for reversible computations. The use of diodes results in relatively simple logic architectures with a small number of control lines. Diodes dissipate energy proportional to their threshold voltage, however, thus placing a lower bound on the efficiency of these circuits. The rank-2 is comprised of circuits in which state 0 or 1 is identical to released state and a certain amount of input information is destroyed during the instruction cycle. The energy dissipated per instruction cycle is proportional to $CV_{\rm t}^2$, where $V_{\rm t}$ is the absolute value of the transistor threshold voltage. Nevertheless, energy dissipation can be reduced appreciably by lowering the rate of change of the driving voltage.

On the other hand, the subthreshold techniques (e.g. [13]–[16]) promise an order of magnitude reduction in power dissipation over above-threshold approach. As the power supply is scaled down, the circuit delay is increased and therefore the subthreshold operation comes at the cost of slower speed. However, subthreshold technique is better suited for ultra low power LSI logic circuits with medium frequency operation.

In recently, the papers which have combined the merits of adiabatic and subthreshold have been presented [12], [17]. In [17] the authors have presented an analytical proof about how sub-threshold charge recovery circuits can meet these characterizations, and then simulated basic blocks as well as a cascaded circuit (i.e., full adder) of some adiabatic logics (e.g., 2N2N2P [3] and SAL [10]) for different voltages, frequencies, and technologies (0.3– 1.1V, 10 kHz– 10 MHz for 65 nm, 90 nm, and 130 nm transistor model). In [12] the authors have focused on dynamic and leakage consumption reductions of charge recovery circuits by using Dual-Threshold CMOS (DTMOS) and gate-length biasing techniques, and then adiabatic computing technique named as p-type effective charge recovery logic (PECRL) has been proposed. However, these papers have been only used predictive technology model (PTM) [18] for simulation, and therefore adiabatic logics in the subthreshold region are not still simulated using a real industrial CMOS process model. Also, they do not make a comparative review of energy dissipation between different adiabatic logics.

In this paper, we report a comparison of energy dissipa-

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tion between different rank-2 quasi-adiabatic logics in the subthreshold operation. In the computer simulation, we use a real industrial 0.18 μm BSIM3v3 model having subthreshold device parameter and confirm the energy savings of quasi-adiabatic logic. The rest of this paper is organized in four sections. The basis of adiabatic and subthreshold operation are presented in Section II and III, respectively. In Section IV we review the simulated adiabatic logics, and then shows that the performance of the adiabatic logics is compared. The conclusions are summarized in Section V.

II. Adiabatic switching

The conventional switching can be understood by using a simple CMOS inverter. The CMOS inverter can be considered to consist of a pull-up and pull-down networks connected to a load (or internal) capacitance C. The pull-up and pull-down networks are actually MOS transistors in series with the same load C. Both transistors can be modeled by an ideal switch in series with a resistor which is equal to the corresponding channel resistance of the transistor in the saturation mode, as shown in Fig. 1(a). When the logic level in the system is "1", there is a sudden flow current through R, where R is equivalent resistance of PMOS pull-up network. A charge $Q = CV_{\rm dd}$ is delivered to the load and the energy which the supply applies is $E_{\rm s} = QV_{\rm dd} = CV_{\rm dd}{}^2$, where $V_{\rm dd}$ is a DC power supply voltage. The energy stored into the load C is a half of the supplied energy:

$$E_{\rm stored} = \frac{1}{2}CV_{\rm dd}{}^2. \tag{1}$$

The same amount of energy is dissipated during the discharge process in the NMOS pull-down network because no energy can enter the ground rail $QV_{\rm gnd} = Q \cdot 0 = 0$. From the energy conservation law, a conventional CMOS logic emits heat and, in this way, it wastes energy in every charge-discharge cycle:

$$\begin{aligned} E_{\rm total} &= E_{\rm charge} + E_{\rm discharge} \\ &= \frac{1}{2}CV_{\rm dd}{}^2 + \frac{1}{2}CV_{\rm dd}{}^2 \\ &= CV_{\rm dd}{}^2. \end{aligned} \tag{2}$$

If the logic is driven by a certain frequency $f\ (= 1/T)$, where T is the period of the signal, then the power of the CMOS gate is determined as:

$$P_{\rm total} = \frac{E_{\rm total}}{T} = CV_{\rm dd}{}^2 f. \tag{3}$$

Adiabatic switching is commonly used to minimize energy loss during charging/discharging. The word "adiabatic" (Greek *adiabatos*, which means impassable) indicates a state change that occurs without heat loss or gain. During adiabatic switching, all the nodes are charged or discharged at a constant current in order to minimize power dissipation. This is accomplished by using AC power supplies to initially charge the circuit during specific adiabatic phases and then discharge the circuit to recover the supplied charge. The principle of adiabatic switching can be best explained by contrasting it with the conventional dissipative switching technique. The

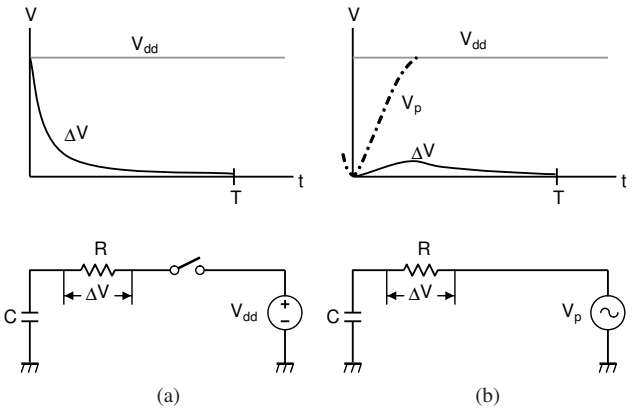

Figure 1. RC tree model. (a) CMOS Charging. (b) Adiabatic Charging.

main idea in the adiabatic switching shown in Fig. 1(b) is that transitions are considered to be sufficiently slow so that heat is not emitted significantly. This is made possible by replacing the DC power supply by a resonance LC driver, an oscillator, a clock generator, etc. If a constant current source delivers the $Q = CV_{\rm dd}$ charge during the time period ΔT, the energy dissipation in the channel resistance R is given by

$$\begin{aligned} E_{\rm diss} &= \xi P \Delta T \\ &= \xi \overline{I}^2 R \Delta T \\ &= \xi \left(\frac{CV_{\rm dd}}{\Delta T} \right)^2 R \Delta T, \end{aligned} \tag{4}$$

where $\overline{I}$ is considered as the average of the current flowing to C, and ξ is a shape factor which depends on the shape of the clock edges. It takes on the minimum value $\xi_{\rm min} = 1$ if the charge of the load capacitor is DC modulated. For a sinusoidal current, $\xi = \pi^2/8 = 1.23$. The above equation indicates that when the charging period ΔT is indefinitely long, in theory, the energy dissipation is reduced to zero. This is called an adiabatic switching.

III. Operation of Subthreshold (or Weak-inversion) Region

Figure 2 shows our measurement result of NMOS transistor $I_{\rm d}$–$V_{\rm gs}$ characteristics for 0.18 μm standard CMOS process. For obtaining this curve, we measured the transistor which has transistor W/L ratio: 1.0 μm/1.0 μm. A closer inspection of the $I_{\rm d}$–$V_{\rm gs}$ curves of Fig. 2(a) reveals that the current is not equal to 0 at $V_{\rm gs} = V_{\rm t}$ (where, $V_{\rm t}$ is threshold voltage of MOS transistor). Because, the MOS transistor is already conducting for voltages below the threshold voltage. This effect is called "subthreshold" or "weak-inversion" conduction. The onset of strong inversion means that ample carriers are available for conduction, but by no means implies that no current at all can flow for gate-source voltages below $V_{\rm t}$. The transition from the on- to the off-condition is thus not abrupt, but gradual. To confirm this effect in somewhat more detail, we again show the $I_{\rm d}$ versus $V_{\rm gs}$ curve on a logarithmic scale as shown in Fig. 2(b). This confirms that the current does not drop to zero immediately for $V_{\rm gs} < V_{\rm t}$, but actually decays in

an exponential fashion, similar to the operation of a bipolar transistor. The current in this region can be approximated by the expression [19]

$$I_{\rm d} = I_{\rm s} e^{\frac{V_{\rm gs}}{nkT/q}} \left(1 - \frac{V_{\rm ds}}{nkT/q}\right), \tag{5}$$

where $I_{\rm s}$ and n are empirical parameters, with $n \gg 1$ and typically ranging around 1.5.

In most digital applications, the presence of subthreshold current is undesirable as it detracts from the ideal switch-like behavior that we like to assume for the MOS transistor. We would rather have the current drop as fast as possible once the $V_{\rm gs}$ falls below $V_{\rm t}$. The inverse rate of decline of the current with respect to $V_{\rm gs}$ below $V_{\rm t}$ hence is a quality measure of a device. It is often quantified by the slope factor S, which measures by how much $V_{\rm gs}$ has to be reduced for the drain current to drop by a factor of 10. From the aforementioned equation, we find the following equation.

$$S = n \left(\frac{kT}{q}\right) \ln(10), \tag{6}$$

where S is expressed in mV/decade. From the measurement results as shown in Fig. 2(b), we find that slope factor: $S = 120$ mV/decade, and $n = 1.67$.

In the subthreshold region, circuits are operated using the minute leakage current, thus resulting in ultra-low power consumption. However, since the driving current decreases exponentially as shown in Fig. 2(b), the delay of the circuit increase sharply. Therefore subthreshold operation of logics can only be applied to limited areas where performance is of secondary importance.

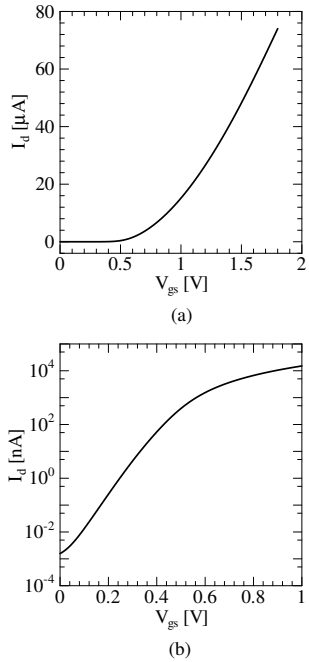

Figure 2. Gate-source voltage ($V_{\rm gs}$) vs. drain current ($I_{\rm d}$) of NMOS device in 0.18 μm CMOS process. (a) $I_{\rm d}$–$V_{\rm gs}$ characteristics. (b) $I_{\rm d}$–$V_{\rm gs}$ in weak inversion.

IV. Comparison of Adiabatic Logic in Subthreshold Region

A. Review of Adiabatic Logic

Figures 3–10 show circuit topology of the various adiabatic logic families. In this subsection we will review advantages and disadvantages of these adiabatic logics.

Figure 3 is 2N2N2P inverter logic reported by Denker [3]. The primary advantage of 2N2N2P is that the cross coupled nMOS transistors result in non-floating output for large part of the recovery phase. The drawback of the 2N2N2P gate is that it requires four phase clocks.

Figure 4 depicts Efficient Charge Recovery Logic (ECRL) [4]. Precharging of this logic is performed with load pMOS transistors and coincides with the generation of output signals, with true and complementary logic signals used simultaneously. Driving is effected with four phase clock pulses. Therefore, ECRL logic will offer high operation speed. The drawback is that it requires push-pull operation and four phase driving, as well as 2N2N2P.

Positive Feedback Adiabatic Logic (PFAL) [5] is shown in Fig. 5. One major difference with respect to 2N2N2P is that functional blocks are in parallel with transmission pMOS. Thus the power dissipation of PFAL becomes small, for the equivalent resistance is smaller when the capacitance needs to be charged. The disadvantage is that PFAL needs four phase driving clocks.

Pass-transistor Adiabatic Logic (PAL) [6] is drawn in Fig. 6. This circuit uses only one-phase sinusoidal clock and therefore circuit topology is very simple. A key disadvantage of this circuitry is that the delay generated from the power supply is increasingly stored in the second and subsequent stages, and thus the operating speed of PAL is lower.

Figure 7 shows Clocked CMOS Adiabatic Logic (CAL) [7]. In order to use one-phase driving, this type of adiabatic logic includes nMOS transistors controlled with ancillary clock pulse: Cx, as shown in Fig. 7. On the other hand, the generation of the ancillary clock (with a frequency divider) means spending more power.

Secure Adiabatic Logic (SAL) [10] is depicted in Fig. 8. This circuit style aims at reducing the data-dependent energy dissipation for security system; thus SAL operates in eight phases and is be complex topology.

Figure 9 indicates an inverter of Two-phase Clocked CMOS Adiabatic Logic (2PC2AL) [11]. The advantage is that it is possible to achieve quasi-adiabatic operation with conventional static CMOS gates under one-phase driving. Therefore circuit topology is the most simple compared with the other adiabatic logics; however the split-level driving clocks are required. On the other hand, the disadvantage is that the output node is be floating from the effect of the split-level driving clocks.

In [12], P-type Efficient Charge Recovery Logic (PECRL) using DTCMOS and gate-length biasing techniques was proposed. In the PECRL circuit as shown in Fig. 10, combinational logic blocks are supplied by a four-phase power clock

and therefore advantage/disadvantage of PECRL is same as ECRL.

B. Simulation Results

To evaluate the operation and the energy dissipation, the adiabatic logic families are tested by SPICE simulation using a 0.18 μm, 1.8 V CMOS standard process technology. The transistor size W/L is 1.0 μm/1.0 μm for all transistors. The voltage of power clock and input signal are taken with 0.5 V, respectively, for adiabatic logics operating in the subthreshold region. In the simulation we assume that the adiabatic logics are implemented on a cryptographic VLSI which is used as a smart card system [9], and therefore the frequency of input signal sets under 10 MHz because ISO/IEC 14443 system uses ASK carrier frequency at 13.56 MHz.

Figure 11 shows a SPICE simulation comparison results of energy consumption for different quasi-adiabatic logic families. The energy dissipation is calculated by integrating the voltage and current product value as follows:

$$E = \int_0^{T_\mathrm{s}} \sum_{i=1}^{n} V_\mathrm{p}^{(i)} I_\mathrm{p}^{(i)} dt, \tag{7}$$

where T_s is the period of the primary input signal; V_p, the power supply voltage; I_p, the power supply current; and n, is the number of power supplies [11]. This result shows that the energy consumption of our previously proposed 2PC2AL is the most smallest compared with other adiabatic logics, in 10 kHz to 10 MHz range.

Table I summarizes the performance comparison of dual-rail quasi-adiabatic logic families. It is apparent from the table that those adiabatic circuits generally suffer from the following conditions (1) multiphase and multiple-clock operations; (2) trapezoid or sinusoidal power clock; (3) interlaced circuit configuration. In this table the main results are summarized as follows: (a) The proposed 2PC2AL circuit is the best suited from the viewpoint of circuit/system structure and energy dissipation, (b) 2PC2AL is also the best suited for logic cell size reduction.

V. Conclusion

In this paper, we have reported a comparison of low-energy adiabatic logic family in the subthreshold operation. In the computer simulation, we have used a real industrial 0.18 μm BSIM3v3 model having subthreshold device parameter and confirmed the energy savings of quasi-adiabatic logic. The simulation result has shown that energy dissipation of our previously proposed 2PC2AL is the most smallest compared with other adiabatic logics, in the frequency range from 10 kHz to 10 MHz.

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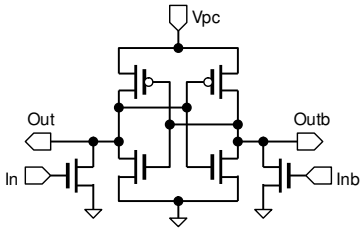

Figure 3. 2N2N2P inverter.

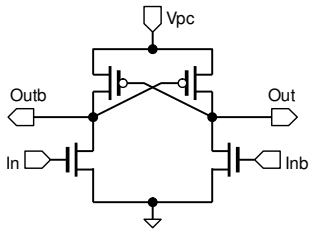

Figure 4. Efficient Charge Recovery Logic (ECRL) inverter.

TABLE I
COMPARISON OF ADIABATIC LOGIC FAMILIES.

	2N2N2P [3]	ECRL [4]	PFAL [5]	PAL [6]	CAL [7]	SAL [10]	2PC2AL [11]	PECRL [12]
Operation clock/phase	4/4	4/4	2/4	2/1(+1)	3/1(+1)	2/8	1/1	4/4
Style for Power clocks	trapezoidal	trapezoidal	trapezoidal	sinusoidal	trapezoidal	trapezoidal	sinusoidal	trapezoidal
Non-adiabatic loss	Y	Y	Y	N	Y	Y	Y	Y
No. of Tr. in inverter	6	4	8	4	8	12	2	4
Energy dissipation	Hi	Hi	Hi	n.a.	Hi	Hi	Low	Hi

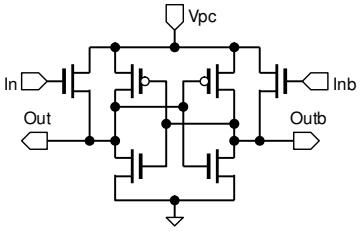

Figure 5. Positive Feedback Adiabatic Logic (PFAL) inverter.

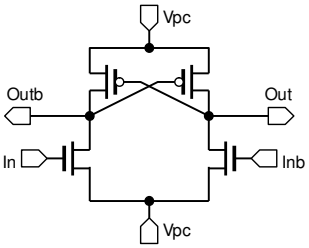

Figure 6. Pass-transistor Adiabatic Logic (PAL) inverter.

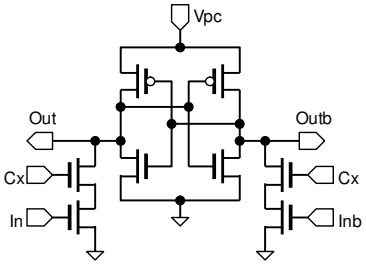

Figure 7. Clocked CMOS Adiabatic Logic (CAL) inverter.

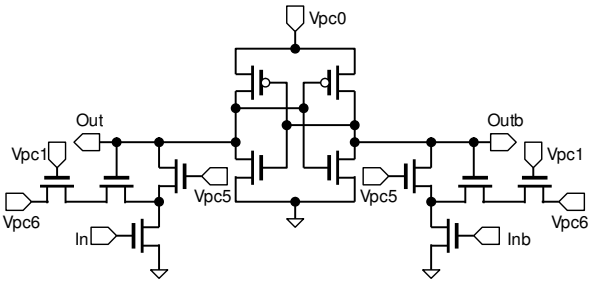

Figure 8. Secure Adiabatic Logic (SAL) inverter.

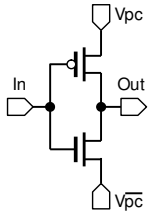

Figure 9. Two-phase Clocked CMOS Adiabatic Logic (2PC2AL) inverter.

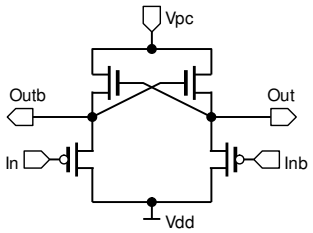

Figure 10. P-type Efficient Charge Recovery Logic (PECRL) inverter.

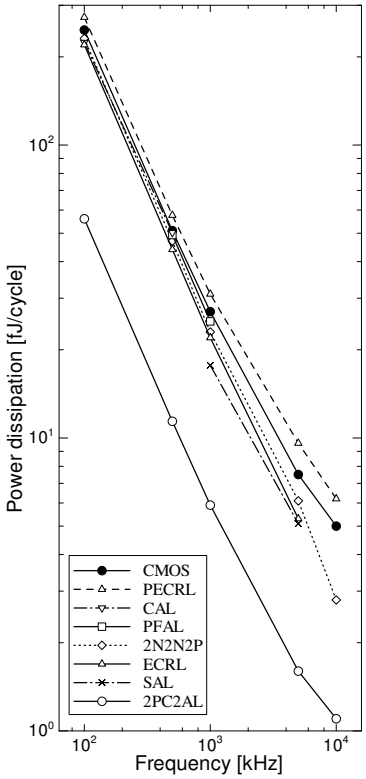

Figure 11. Energy consumption of different adiabatic logics. Note that PAL is not fully operated in the subthreshold region.