2PASCL: Energy dissipation of NAND circuit using new split level driving value and CMOS bulk connection

Nazrul Anuar

Graduate School of Eng., Gifu University

Abstract

This paper proposes a new quasi adiabatic logic family that uses two complementary pulsed supply clock for digital low power applications such as sensors. The proposed two-phase adiabatic static CMOS logic circuit (2PASCL) has switching activity that is lower than dynamic logic and can be directly derived from static CMOS circuits. We have done a SPICE simulation on the 2PASCL NAND implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the gates. This circuit is emphasis on the recycle of the charges as two diodes are placed for the discharging. The ealier results of inverter logic, it shows that 2PASCL can save a maximum of 63.3% of power dissipation over static CMOS logic at transition frequencies of 50MHz to 100MHz.

1 Introduction

The differences compared to static CMOS NAND circuit are two diodes placed near the output and next to the nMOS logic and clocking voltage power supply to replace the V_{dd} and the GND. Then by using the SPICE simulation, the energy dissipation for one cycle is calculated. The energy in joule is then converted to watt by multiplying it with the input frequency.

In the previous simulation, the functional of 2PASCL as NAND logic circuit has been confirmed by using split level driving and the results have been compared to two phase inverted pulse. Split level driving produced better output waveforms which clearly differentiate the Hi and Lo signal. However the energy dissipation is higher when using split level pulse. As for trapezoidal driving voltage, we have also done a simulation on the T_{rise}, T_{fall}. The slower the rise and the fall time, the lower the energy dissipation. We still need to further study 2PASCL as the energy dissipation at frequency of 10 to 100 MHz is still higher compared to CMOS.

In this paper, we are going to use the input pulse voltage with the height of 1.8V. The driving pulse is the split level of trapezoidal which is 4 times the speed of the input signal. The range of the split level pulse is 0 to 1.8V. We will simulate the circuit by connecting the bulk (substrate) of pMOS to the $V\phi$, V_{dd} and nMOS to $\overline{V\phi}$, V_{ss} and the results will be compared to the existing way to connect the bulks.Then we will again compare the trapezoidal, sinusoidal driving voltage energy dissipation to the static CMOS logic NAND circuit which V_{dd} is 1.8V.

2 Simulation and results

The simulation of 2PASCL NAND circuit as in schematic diagram shown in Fig. 1–3 which showing different bulk connection legs has been done using the circuit data as shown in Table 1 . The simulation result for the transition frequency of 10 to 100 MHz is shown in Fig.4. From the result, we understand that there is no significant difference when changing the CMOS bulk connections. However for leg 3, at 100 MHz, we can see a slight lower energy dissipation compared to leg 1 and 2.

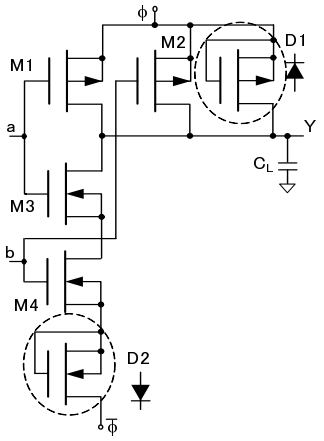

Fig. 1 Leg 1: NAND logic circuit with 2PASCL configuration. nMOS and pMOS connected as existing.

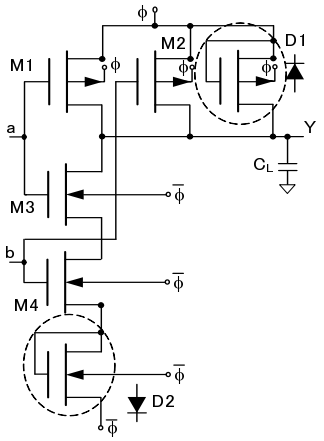

Fig. 2 Leg 2: NAND logic circuit with 2PASCL configuration. nMOS bulk connected to $\overline{\phi}$ and pMOS bulk to ϕ.

Table 1 Circuit data

Driving power	-1.2–1.2V
C_L	0.1 pF
Diodes	W/L : 0.6μm/0.18μm
nMOS, pMOS	W/L : 0.6μm/0.18μm
T_{rise} and T_{fall}	0.6ns (trapezoidal)

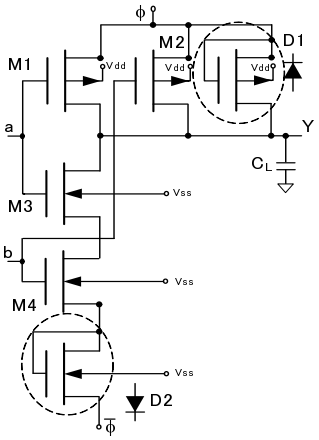

Fig. 3 Leg 3: NAND logic circuit with 2PASCL configuration. nMOS bulk connected to Vss and pMOS bulk to Vdd.

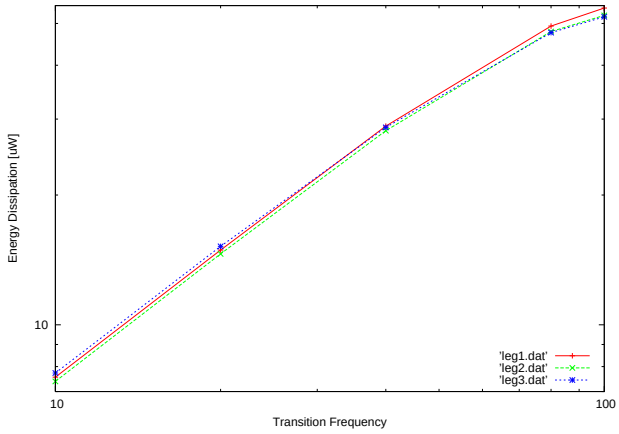

Fig. 4 NAND logic energy dissipation comparison between leg 1,2 and 3.

For the next simulation, we use split driving pulse ranging from 0 to 1.8V. Previously we had used the range of -1.2 to 1.2V. Sinusoidal and trapezoidal at 10, 20, 40, 80 and 100 MHz is compared to the same frequency of CMOS static NAND logic circuit. We use the circuit data as shown in Table 2. We use leg 3 connection as the result at 100 MHz shows slightly lower energy dissipation compared to leg 1 and 2. The result is shown in Fig. 5. In Fig. 6, we have confirmed the output waveforms of sinusoidal split driving voltage at 100 MHz transition frequency. The delay time from input to output measured as 1.28 ns. At 100 MHz, by using leg 3, the energy dissipation is 1.17μW compared to 1.25μW when using leg 2. From the comparison result, sinusoidal split driving voltage with 1.8V peak can reduced a maximum of 30.5% from the transition frequency of 10 to 100 MHz of NAND logic configured with 2PASCL circuit.

Table 2 Circuit data for sinusoidal, trapezoidal and static CMOS comparison

Driving power voltage	0–1.8V
Split level	0–0.9V, 0.9–1.8V
Freq, (input: driving voltage)	1:4
C_L	0.01 pF
Diodes	W/L : 0.6μm/0.18μm
nMOS, pMOS	W/L : 0.6μm/0.18μm
T_{rise} and T_{fall}	0.6ns (trapezoidal)

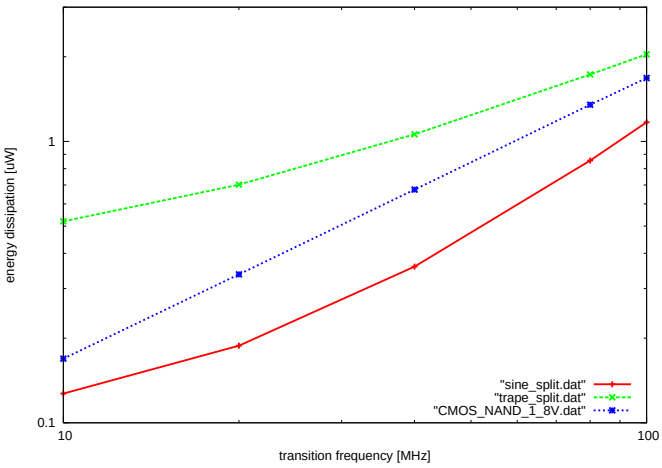

Fig. 5 NAND logic circuit with split level.

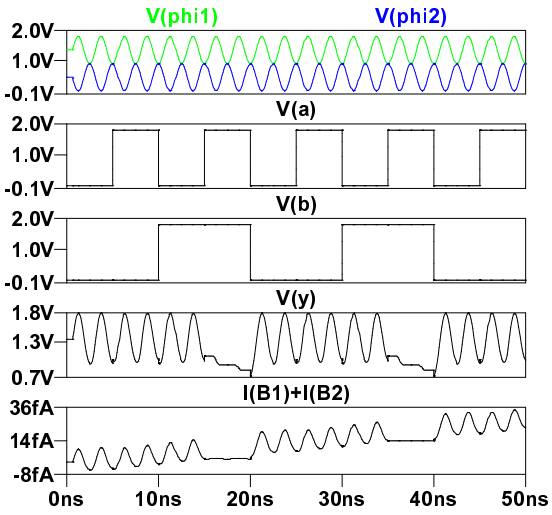

Fig. 6 NAND logic circuit with 2 phase inverted.

3 Conclusion

In this simulation, sinusoidal using split level dissipates lower energy compared to trapezoidal driving voltage. This is just the opposite when using the two phase inverted driving pulse. By using split level driving voltage and bulks connection to the V_{dd} and V_{ss}, we managed to produce a better output waveforms and significantly lower energy dissipation. It is 30.5% lower when using 2PASCL NAND logic compared to static

CMOS NAND logic with the V_{dd} of 1.8V.