4-bit Ripple Carry Adder using Two Phase Clocked Adiabatic Static CMOS Logic

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***Abstract*—This paper demonstrates the low energy operation of 4-bit ripple carry adder (RCA) employing two phase clocked adiabatic static CMOS logic (2PASCL) circuit techniques. We evaluate NOT, NAND, XOR and NOR logic gates on the basis of the 2PASCL topology using SPICE implemented using 0.18 μm CTX CMOS technology. For NOT circuit, analytical and simulation values are compared. By removing the diode from the charging path, higher output amplitude is achieved and the power consumption of the diode is eliminated. From the simulation results, we find that 4-bit 2PASCL RCA can save an average of 71.3% of dissipated energy as compared to that with a static 4-bit CMOS RCA at transition frequencies of 10 to 100 MHz. The results indicates that 2PASCL technology can be advantageously applied to low-power digital devices operated at low frequencies, such as radio-frequency identifications (RFIDs), smart cards, and sensors.**

I. Introduction

With the widespread use of mobile and wireless devices and the increase of clock and logic speeds to meet the new performance requirements, energy efficiency has become a key design aspect in the field of integrated circuits (ICs). For digital circuits, which mostly utilize complementary metal-oxide-semiconductor (CMOS), voltage scaling is one of the main strategies as the power consumption is proportional to the square of the power supply voltage. To achieve a high transistor drive current and thereby improve the circuit performance, the transistor thresholds must be scaled down in proportion to the supply voltage. However, scaling down of the transistor threshold voltage, V_t results in significant increase in subthreshold leakage current [1].

In recent years, studies on adiabatic computing have been utilized for low-power systems and several adiabatic logic families have been proposed [2]– [9]. However, we have observed several weaknesses of the diode based logics such as low output amplitude and the power dissipation of the diodes at the charging path.

In this study, we design and simulate a 4-bit ripple carry adder (RCA) [10] using 2PASCL [11] topology and compare its power consumption per cycle to CMOS RCA. Prior to that, we simulate and compare the power consumption of NOT, NAND, XOR and NOR logics using 2PASCL and CMOS circuit technologies. We choose RCA as it has a longer propagation path than other do adders.

A novel method for reducing the power dissipation in a 2PASCL circuit involves; the design of a charging path without diodes. In such a case, current flows only through the transistor during the charging. Thus, a 2PASCL circuit is different from other diode-based adiabatic circuits, in which current flows through both the diode and transistor. By using the aforementioned 2PASCL circuit, we can achieve high output amplitudes and reduce power dissipation. In addition, in order to minimize the dynamic power consumption in this circuit, we apply a split-level sinusoidal driving voltage.

II. CMOS vis-a-vis Adiabatic Logic

A. CMOS

Power dissipation in conventional CMOS circuits primarily occurs during device switching. As shown in Fig. 1, both pMOS and nMOS transistors can be modeled by including an ideal switch in series with a resistor in order to represent the effective channel resistance of the switch and the interconnect resistance. The pull-up and pull-down networks are connected to the node capacitance C_L, which is referred to as the load capacitance in this paper.

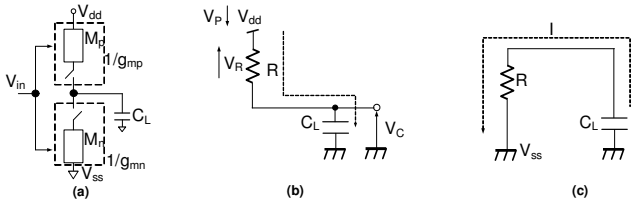

Fig. 1. (a) A CMOS model showing an ideal switch in series with resistor. (b) Charging. (c) Discharging.

When the logic level in the system is "1," there is a sudden flow of current through R. $Q = C_L V_{dd}$ is the charge supplied by the positive power supply rail for charging C_L to V_{dd}. Hence, the energy drawn from the power supply is $Q \cdot V_{dd} = C_L V_{dd}^2$ [3]. If it is assumed that the energy drawn from the power supply is equal to that supplied to C_L, the energy stored in C_L becomes one-half the supplied energy, i.e., $E_{stored} = (\frac{1}{2})C_L V_{dd}^2$. The remaining energy is dissipated in R. The same amount of energy is dissipated during discharging in the nMOS pull-down network when the logic level in the

system is "0." Therefore, the total amount of energy dissipated as heat during charging and discharging is:

$$E_{charge} + E_{discharge} = \frac{1}{2} C_L V_{dd}^2 + \frac{1}{2} C_L V_{dd}^2 = C_L V_{dd}^2. \quad (1)$$

From the above equation, it is apparent that the energy consumption in a conventional CMOS circuit can be reduced by reducing V_{dd} and/or C_L. By decreasing the switching activity in the circuit, the power consumption ($P = \frac{dE}{dt}$) can also be proportionally suppressed.

B. Adiabatic Logic

Adiabatic switching is commonly used to minimize energy loss during charging/discharging. The word "adiabatic" (Greek *adiabatos*, which means impassable) indicates a state change that occurs without heat loss or gain. During adiabatic switching, all the nodes are charged/discharged at a constant current in order to minimize power dissipation. This is accomplished by using AC power supplies to first charge the circuit during specific adiabatic phases and then discharge the circuit to recover the supplied charge.

The principle of adiabatic switching can be best explained by contrasting it with the conventional dissipative switching technique. Figure 2 shows the manner in which energy is dissipated during a switching transition in adiabatic logic circuits. As opposed to the case of conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the used of a time-varying voltage source instead of a fixed voltage supply.

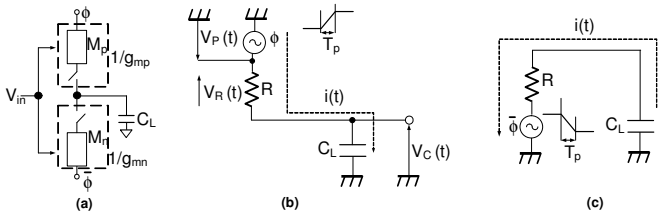

Fig. 2. (a) Model of adiabatic logic showing an ideal switch in series with resistance and two complementary voltage supply clocks. (b) Charging. (c) Discharging.

The peak current in adiabatic circuits can be significantly reduced by ensuring uniform charge transfer over the entire available time. Hence, if $\hat{I}$ is considered as the average of the current flowing to C_L, the overall energy dissipated during the transition phase can be reduced in proportion as follows:

$$\hat{I}^2 R T_p = \left(\frac{C_L V_{dd}}{T_p}\right)^2 R T_p = \left(\frac{R C_L}{T_p}\right) C_L V_{dd}^2. \quad (2)$$

Theoretically, during adiabatic charging, when the time for the driving voltage ϕ to change from 0 V to V_{dd}, T_p is long, power dissipation is nearly zero.

When $\overline{\phi}$ changes from HIGH to LOW in the pull-down network, discharging via the nMOS transistor occurs. From Eq. (2), it is apparent that when power dissipation is minimized by decreasing the rate of switching transition, the system draws some of the energy that is stored in the capacitors during a given computation step and uses it in subsequent computations. It must be noted that systems based on the abovementioned theory of charge recovery are not necessarily reversible.

III. 2PASCL

A. Circuit Operation

Figure 3 shows a circuit diagram and waveforms illustrating the operation of the 2PASCL inverter [11]. A two-diode circuit is used, one diode is placed between the output node and power clock, and the other diode is placed adjacent to the nMOS logic circuit and connected to another power source. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. Such a circuit design is particularly advantageous if the signal nodes are preceded by a long chain of switches.

The proposed system uses a two-phase clocking split-level sinusoidal power supply, wherein ϕ and $\overline{\phi}$ replace V_{dd} and V_{ss}, respectively. One clock is in phase while the other is inverted. The voltage level of ϕ exceeds that of $\overline{\phi}$ by a factor of $V_{dd}/2$. By using these two split-level sinusoidal waveforms, which have peak-to-peak voltages of 0.9 V, the voltage difference between the current-carrying electrodes can be minimized, consequently power consumption can be suppressed. The substrates of the pMOS and nMOS transistors are connected to ϕ and $\overline{\phi}$ respectively.

Since the criteria for maintaining thermal equilibrium, in which the voltage between the current-carrying electrodes is zero when the transistors are in the ON state [4] are satisfied, the energy accumulated in C_L is not dissipated. The results of the simulation performed using a "simulation program with the integrated circuit emphasis (SPICE)" circuit simulator reveal that adiabatic circuits powered by split-level sinusoidal waveforms consume less energy than a trapezoidal clock power supply, even if the rise and fall times of the trapezoidal waveforms are set to their maximum values. Moreover, sinusoidal waveforms can be generated with a higher energy efficiency than trapezoidal waveforms [7].

The circuit operation is divided into two phases, *evaluation* and *hold*. In the *evaluation* phase, ϕ swings up and $\overline{\phi}$ swings down. On the other hand, in the *hold* phase, $\overline{\phi}$ swings up and ϕ swings down. Let us consider the inverter logic circuit demonstrated in Fig. 3. The operation of the 2PASCL inverter is explained as follows.

1) *Evaluation* phase:
   a) When the output node Y is LOW and the pMOS tree is turned ON, C_L is charged through the pMOS transistor; hence, the output is in the HIGH state.
   b) When node Y is LOW and nMOS is ON, no transition occurs.
   c) When the output node is HIGH and the pMOS is ON, no transition occurs.
   d) When node Y is HIGH and the nMOS is ON, discharging via nMOS and D2 causes the logic state of the output to be "0" [9].

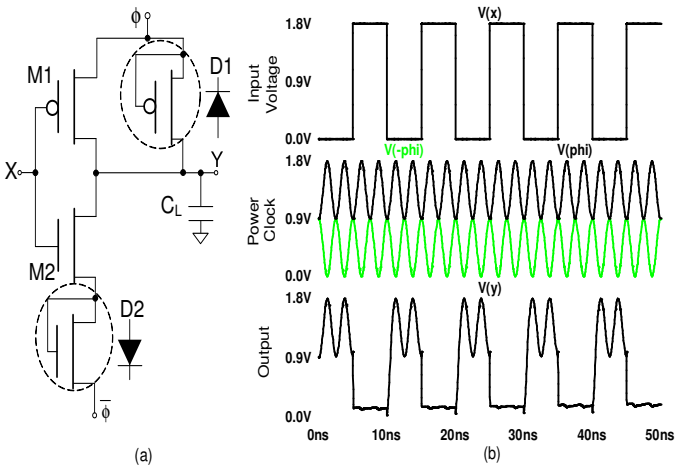

Fig. 3. (a) 2PASCL inverter circuit. (b) Waveforms from the simulation, transition frequency X=100 MHz, ϕ = $\overline{\phi}$ = 400 MHz.

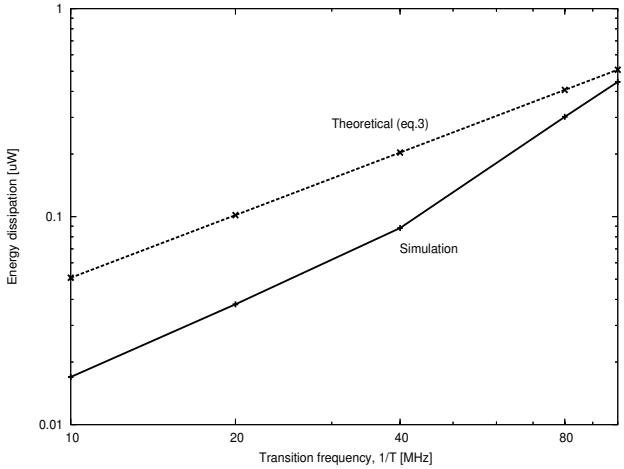

Fig. 4. Power dissipation per cycle comparison of the simulation results and theoretical values of 2PASCL-based inverter gate.

2) *Hold* phase:
   a) When node Y is LOW and the nMOS is ON, no transition occurs.
   b) At the point when the preliminary state of the output node is HIGH and the pMOS is ON, discharging via D1 occurs.

The number of dynamic switching transition occuring during the operation of the 2PASCL circuit decreases since the charging/discharging of the circuit nodes does not necessarily occur during every clock cycle. Hence, node switching activities are suppressed to a significant extent and consequently, energy dissipation is also reduced. One of the advantages of the 2PASCL circuit is that it can be made to behave like a static logic circuit.

B. Theoretical Analysis

In adiabatic circuits, energy dissipation occurs through the threshold voltage and transistor channel resistance. To estimate the energy consumption in adiabatic circuits, we utilize an RC model with a threshold voltage V_t. The energy dissipation in a 2PASCL inverter is as follows:

$$\begin{aligned} E_{2PASCL} &= E_{chrg(M1)} + E_{dischrg(D1)} + E_{dischrg(M2,D1)} \\ &= \frac{1}{2}C_L V_{tp}^2 + \frac{1}{2}C_L V_{\phi p-p} \mid V_{tp} \mid + \frac{1}{2}C_L (V_{\overline{\phi} p-p} - V_{tn}) V_{tn} \\ &= \frac{1}{2}C_L \left(V_{tp}^2 + V_{\phi p-p} \mid V_{tp} \mid + (V_{\overline{\phi} p-p} - V_{tn}) V_{tn} \right), \quad (3) \end{aligned}$$

where C_L is the load capacitance; V_{tp} the threshold voltage of pMOS; V_{tn} the threshold voltage of nMOS; and $V_{\phi p-p}$ and $V_{\overline{\phi} p-p}$ the voltage supplies.

By assuming C_L=0.01 pF, $\mid V_{tp} \mid$=0.58 V, V_{tn}=0.24 V, and $V_{\phi p-p}$ = $V_{\overline{\phi} p-p}$= 0.9 V, the theoretical calculations are plotted. As shown in Fig. 4, the power dissipation at each transition frequency is compared. The unmatched values of the simulation and analytical results are primarily because of the shape factor of voltage drivers which are not considered in the theoretical calculations. However, we have understood the fundamental factors that contributed to the power dissipation in the 2PASCL inverter from this analytical analysis. From Eq. 3, by applying $V_{\phi p-p}$ and $V_{\overline{\phi} p-p}$ as split-level sinusoidal waveforms, with each peak-to-peak voltage being 0.9 V, we have saved approximately 50% of the energy, as compared to non-split-level waveforms.

C. Inverter Circuit

1) Simulation Condition: The paper starts by examining the logic function and power dissipation of a simple 2PASCL gate, which is an inverter. The simulations in this study were performed using a SPICE circuit simulator with a 0.18 μm, 1.8-V CTX CMOS process. The width W and length L of the nMOS and pMOS logic gates were 0.6 μm and 0.18 μm, respectively. A capacitive load C_L, of 0.01 pF is placed at the output node Y. The frequency of power supply clock is set to be exactly four times higher than the transition frequency.

2) Simulation Results: The SPICE simulation results obtained for the 2PASCL inverter are shown in Fig. 3 (b). The top graph demonstrates the input signal which is a CMOS-compatible rectangular pulses. The middle graph shows the driving voltage of the split-level sinusoidal supply clock, and the last graph shows the output waveform. The energy dissipation is calculated by integrating the product of voltage and current as follows:

$$E = \int_0^T \left(\sum_{i=1}^{n} (V_{pi} \times I_{pi}) \right) dt, \quad (4)$$

where T is the period of the primary input signal; V_p, the power supply voltage; I_p, the power supply current; and n, is the number of power supplies [9]. The energy in joule is then converted to watt by multiplying it with the input frequency.

a) Comparison of power dissipation: The graph shown in Fig. 5 (top) reveals that with the 2PASCL inverter, up to 97% of the power dissipated from the CMOS inverter can

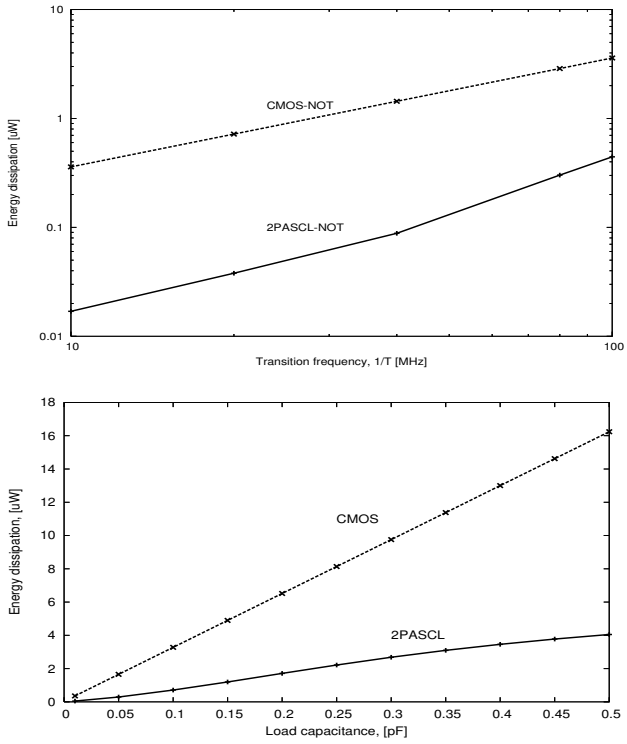

Fig. 5. Energy comparison of 2PASCL inverter with CMOS at transition frequencies of 10 MHz to 100 MHz (top), and load capacitance from 0.01 pF to 0.5 pF (bottom).

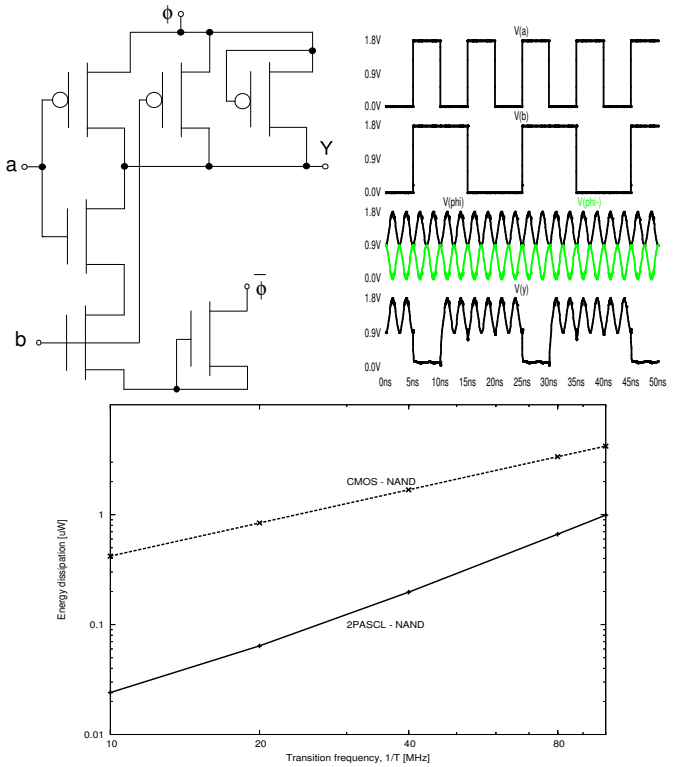

Fig. 6. Scheme for 2PASCL-based NAND logic (top left), waveforms from the simulation at X=100 MHz where the output $Y = \overline{a \cdot b}$ (top right), and power dissipation compared to conventional NAND gate (bottom).

be saved. Previous results [11] also show that the 2PASCL inverter offers the lowest power dissipation among all the other adiabatic inverter logic circuits.

b) Power dissipation at different value of C_L: The simulation results show that the power dissipation in the 2PASCL inverter is 63% lower than that of CMOS static when the C_L values are changed from 0.01 to 0.5 pF, as shown in Fig. 5 (bottom).

IV. Applications of Proposed Circuit

A. Combination Logic Circuit

The first combination circuit examined in this study is NAND logic. Our proposed schematic is shown in Fig. 6. The logic function of the circuit as shown on the right graph is confirmed. From the comparison study with CMOS, we find that a 2PASCL-based NAND circuit can save up to 30.5% at transition frequencies of 10 to 100 MHz.

We then simulated two combination logic circuits; 2PASCL-based XOR and NOR circuits. Both the schematics are demonstrated in Fig. 7 and Fig. 8. By using the split-level sinusoidal driving clocks, the proposed XOR and NOR have 68% and 26% lower energy than conventional static CMOS, respectively. As shown in Fig. 7, the scheme for a 2PASCL XOR has no diodes at the output Y. The discharging diodes of pMOSs are placed only at the inverter site of the circuit. However, in the case of an nMOS diode, it remains adjacent to the nMOS logic circuit and $\overline{\phi}$. As for the result of XOR, at transition frequency above 70 MHz, the power dissipation of CMOS is lower than 2PASCL XOR. This suggests the optimum transition frequency of the 2PASCL XOR to achieve low-power dissipation.

B. 4-bit Ripple Carry Adder

1) Simulation Condition: To verify the practical applicability of the proposed 2PASCL circuit, we design and simulate a 4-bit RCA (Fig. 9). As illustrated in Fig. 10, each full adder (FA) consists of NAND and XOR gates. To enhance the accuracy of performance evaluation, we simulate the frequency characteristics of power consumption for the RCA of the 2PASCL circuit and compare the results with those obtained for the CMOS RCA circuit. We record the power dissipation values at the same time period for both these circuits.

2) Simulation Results: We also confirm the functionality of the 4-bit 2PASCL RCA circuits as demonstrated in Fig. 11 (top). The results (Fig. 11) show that lesser power dissipation occurs in the 2PASCL circuit with the split-level sinusoidal clocking voltage than in the conventional static CMOS RCA. Further, it is apparent that power dissipation is very less in the 2PASCL RCA when the simulated transition frequency is 10–100 MHz as shown in the same figure.

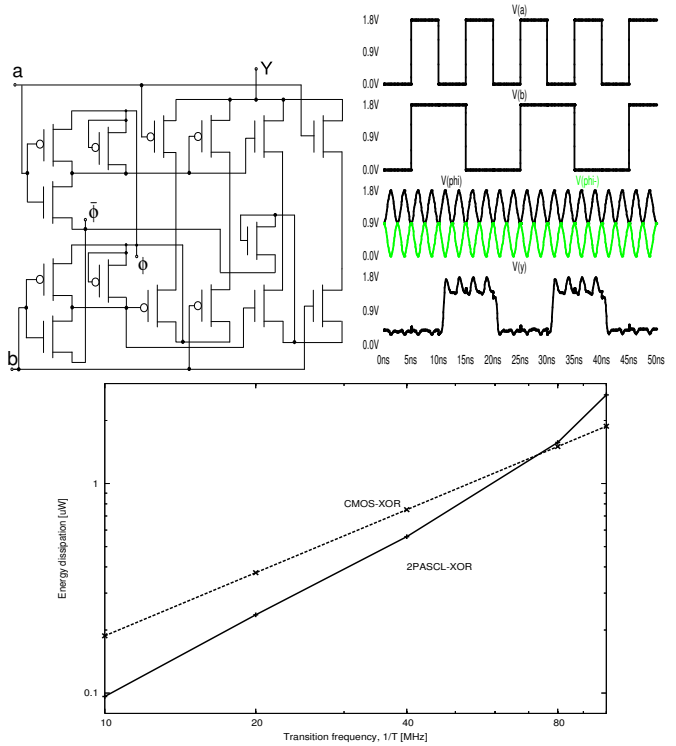

Fig. 7. Scheme for 2PASCL-based XOR logic (top left), and waveforms from the simulation at X=100 MHz where the output $Y = a \oplus b$ (top right), and power dissipation compared to conventional XOR gate (bottom).

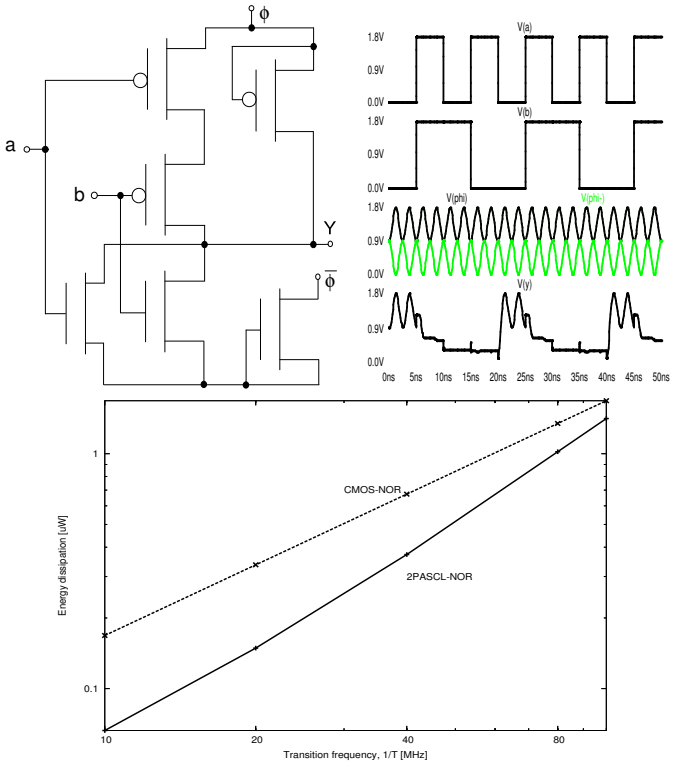

Fig. 8. Scheme for 2PASCL-based NOR logic (top left), and waveforms from the simulation at X=100 MHz where the output $Y = \overline{a + b}$ (top right), and power dissipation compared to conventional NOR gate (bottom).

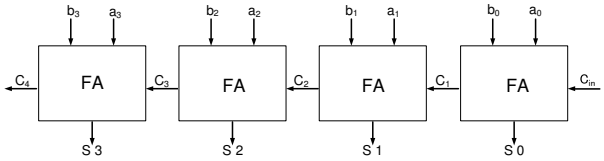

Fig. 9. 4-bit Ripple carry adder (RCA).

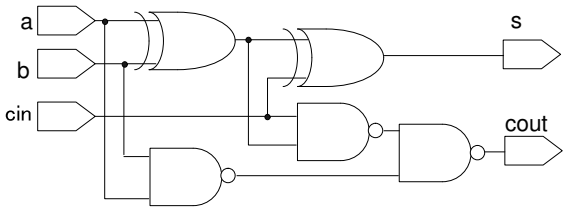

Fig. 10. Logic structure of a full adder.

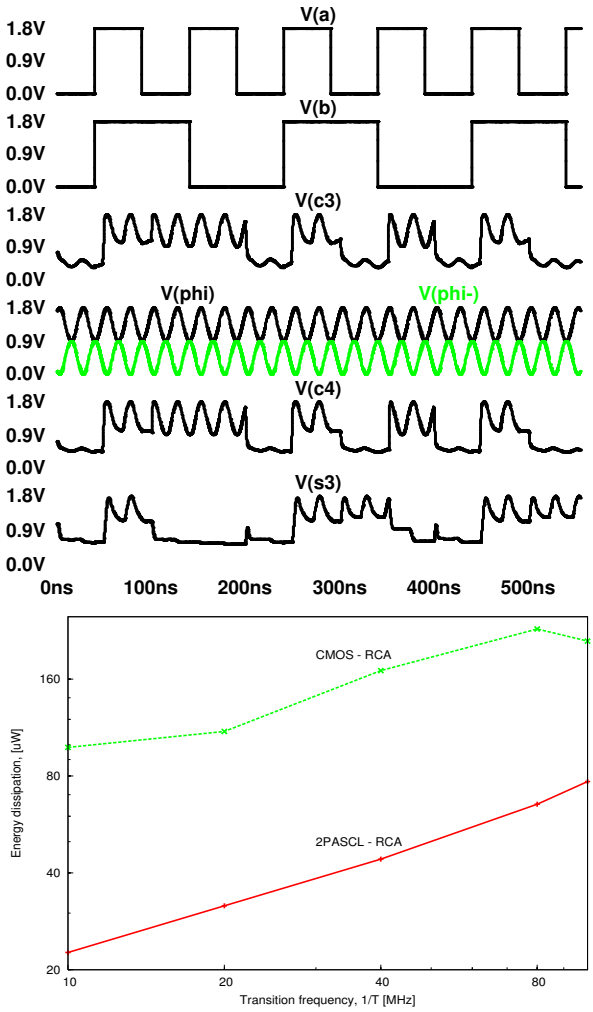

Fig. 11. Output waveforms for 4-bit ripple carry adder (RCA) of 2PASCL from the simulation result (top), and power dissipation of RCAs per cycle over frequency (bottom).

V. Discussion

While the 2PASCL circuit has advantages such as low power dissipation and high fan-out, its main disadvantage is floating outputs, which are attributed to the alternate hold phases that exist during the circuit operation. Furthermore, there is a risk of current leakage (although small) since the gates are slowly switched ON. These problems will be addressed in our future research. The configuration of the two complementary low-power split-level sinusoidal power supply clocks is not discussed in this paper. The design of the power supply circuit will be proposed in a future study.

VI. Conclusion

In this paper, we have described the simulation of a 4-bit 2PASCL ripple carry adder (RCA) and its comparison with a CMOS RCA on the basis of adiabatic charging and energy recovery. When the input frequency is 10–100 MHz, the 2PASCL RCA dissipates a minimum of 28.7% of the energy dissipated by a static CMOS RCA. The simulation results show that power consumption in the 2PASCL NOT, NAND, XOR, and NOR circuits are considerably lesser than that in a CMOS. Further, the energy dissipated by a 2PASCL inverter remains low even when the load capacitance is increased. We believe that the proposed adiabatic logic circuits is advantageous for ultra-low-energy computing applications.

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